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Letter

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Planar Edge Schottky Barrier-Tunneling Transistors Using Epitaxial Graphene/SiC Junctions

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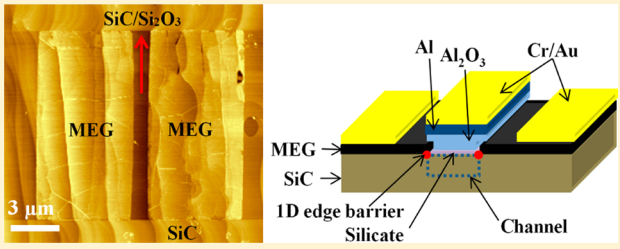
Supporting Information

ABSTRACT: A purely planar graphene/SiC field effect transistor is presented here. The horizontal current flow over one-dimensional tunneling barrier between planar graphene contact and coplanar two-dimensional SiC channel exhibits superior on/off ratio compared to conventional transistors employing vertical electron transport. Multilayer epitaxial graphene (MEG) grown on SiC(000$\bar{1}$) was adopted as the transistor source and drain. The channel is formed by the accumulation layer at the interface of semi-insulating SiC and a surface silicate that forms after high vacuum high temperature annealing. Electronic bands between the graphene edge and SiC accumulation layer form a thin Schottky barrier, which is dominated by tunneling at low temperatures. A thermionic emission prevails over tunneling at high temperatures. We show that neglecting tunneling effectively causes the temperature dependence of the Schottky barrier height. The channel can support current densities up to 35 A/m.



KEYWORDS: *Epitaxial graphene, semi-insulating silicon carbide, Schottky barrier transistor, space-charge-limited current, tunneling field effect transistor*

Graphene has been widely considered as a candidate for next generation electronics due to its exceptional electronic, mechanical, and optical properties.[1,2] Logic transistors[3] and high frequency transistors[4,5] have been demonstrated using the high electron mobility in graphene. However, the fact that graphene lacks band gap presents an obstacle to achieve large on/off ratio. Many efforts, such as quantum confinement,[6] applying a perpendicular electrical field,[7] and chemical functionalization,[8] have been made to open a band gap in graphene, but it is difficult to maintain high mobility while converting graphene into a semiconductor. Alternative approaches including vertical tunneling transistor structures,[9] graphene/semiconductor MESFETs,[10] and graphene Schottky barrier diodes[11] have been explored and shown significant improvement in the current on/off ratio. Solid state three-terminal devices that mimic the performance of triodes by tuning Fermi level in graphene have been also investigated.[12] Epitaxial graphene on the C-face of semi-insulating SiC has a unique advantage for the integration of graphene electronics and SiC semiconducting properties.[13] C-face multilayer epitaxial graphene can withstand high temperatures and is a very good conductor.[14] Wide band gap SiC has also attracted increasing attention due to its high breakdown field, high thermal conductivity, and high saturation drift velocity,[15] and the SiC MOSFET is considered as a promising candidate for low-loss and fast power devices.[16] C-face SiC develops into a variety of surface reconstructions upon high temperature annealing,[17,18] which can be used to tailor properties of SiC/graphene or SiC/oxide interface.

In this letter, we present fabrication and operation of a Schottky barrier transistor, which combines advantages of both graphene and SiC. The transistor exhibits up to 2 orders of magnitude higher on/off ratio than the most recent field effect transistors[10] and triodes.[12] We use semi-insulating 6H-SiC substrate (from II−VI incorporated, vanadium doped) and confinement controlled sublimation growth and annealing method.[19] A graphene-SiC-graphene Schottky barrier transistor structure is sketched in Figure 1d. It was fabricated by multiple e-beam lithography patterning, oxygen plasma etching, and two high temperature annealing steps as described below; see Supporting Information for details. A MEG is grown during the first annealing step. Then source and drain contacts are defined lithographically, followed by the conduction channel formation by high quality SiC/silicate interface at the second high temperature annealing. The sample surface has been oxygen etched everywhere except for the channel in order to avoid

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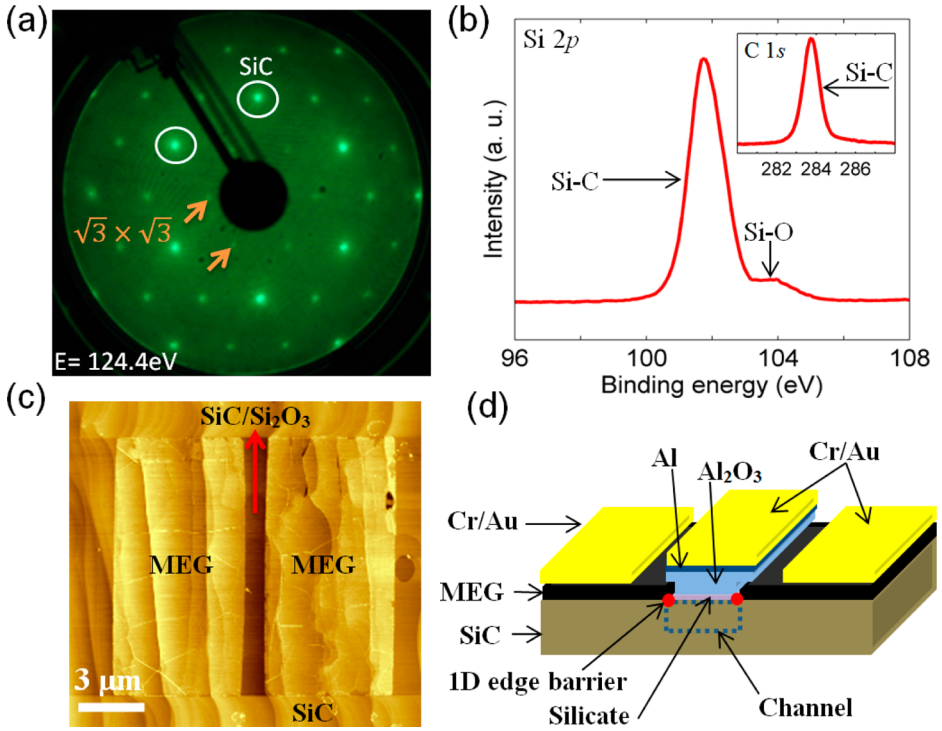

Figure 1. (a) LEED pattern of high temperature annealed C-face SiC demonstrates $\sqrt{3} \times \sqrt{3}R30°$ pattern, as indicated by orange arrows and labels. White circles show SiC bulk (1 × 1) diffraction spots. (b) Si2p core level spectrum; (inset) C1s core level spectrum. (c) AFM topography of high temperature annealed SiC with multilayer epitaxial graphene stacks as contacts. (d) Schematic diagram of a finished Schottky barrier transistor with a top gate. The positions of the accumulation layer and the one-dimensional edge Schottky barrier are marked by dotted blue rectangle and two red dots, respectively.

interdevice parasitic conductance. The annealed C-face SiC surface was characterized by low energy electron diffraction (LEED) and X-ray photoelectron core level spectroscopy (XPS). Figure 1a is the LEED pattern for the high temperature annealed C-face SiC surface. It shows a $\sqrt{3} \times \sqrt{3}R30°$ surface reconstruction related to the SiC bulk (1 × 1) spots. The chemical elemental composition of the surface material was studied by the XPS core level spectra, see Figure 1b. Both LEED and XPS results suggest presence of an ordered thin silicate (Si_2O_3) layer on the surface of the high temperature annealed C-face SiC (Supporting Information).[20,21]

The band bending voltage V_b at the interface can be derived from the binding energy (E_B) of the peak associated with the C−Si bond in the XPS C1s spectra, see Figure 1b. The XPS data analysis gives a surface electron electrostatic energy for the semi-insulating 6H-SiC and Si_2O_3 interface (−0.6 ± 0.1) eV. A similar experiment and analysis was done on the 6H-SiC and multilayer epitaxial graphene interface giving a band bending electron energy of +0.7 ± 0.1 eV with SiC band bent upward (Supporting Information). The surface potential energy −0.6 eV at the SiC/Si_2O_3 interface brings the SiC conduction closer to the Fermi level, which leads to the accumulation of electrons in the conduction band.[22]

The formation of the conducting accumulation layer has been also modeled (Supporting Information) by self-consistent solution of Poisson and Schrödinger equation taking into account positively charged donors, negatively charged acceptors, free charge in the channel, gap states on SiC/Si_2O_3 interface, and spontaneous polarization of hexagonal 6H-SiC polytype. The density of interface states D_{it} was the only unknown parameter. In order to reproduce correctly the formation of the accumulation layer, D_{it} has to be sufficiently low ($D_{it} = 3 \times 10^{12}$ cm^{-2} eV^{-1}). This confirms the conclusion that the silicate add-layer forms a well-defined interface between SiC and gate oxide just as SiO_2 forms a well-defined interface between silicon and gate oxide in silicon electronics. The silicate layer is therefore essential in providing low density of interface states thus unpinning the Fermi level and allowing formation of the accumulation layer, unlike the case of disordered SiC/oxide interface.

The device before top gate deposition was characterized by atomic force microscopy (AFM) and Raman scattering spectroscopy confirming the absence of graphene in the channel. Figure 1c is the AFM image after high temperature annealing where multilayer epitaxial graphene contacts and SiC/Si_2O_3 areas can be seen. The channel area (the darkest area in Figure 1c) is deeper than the SiC substrate around the device due to the formation of amorphous SiO_2 during second oxygen etching. Figure 1d schematically shows a side view of the device after depositing metal (Au/Cr) contacts and Al/Al_2O_3 top gate.

The device electrical characterization is presented below and interplay of thermionic emission and tunneling at the channel/graphene edge is analyzed. Figure 2a is a schematic diagram for the transport setup. The zero gate voltage DC performance of a MEG-[SiC/Si_2O_3]-MEG device with L = 900 nm channel length is shown in Figure 2b. An exponential increase in the low source/drain current region with respect to source/drain voltage is observed. The energy band diagram at different drain-source bias is shown at V_{DS} = 0 V, V_{DS} > 0 V, and V_{DS} < 0 V (inset of Figure 2b). Considering the band bending voltage at the SiC/MEG (+0.7 V) and SiC/Si_2O_3 (−0.6 V) interface, the device can be modeled as back-to-back Schottky diodes connected by a conduction channel (band schemes in Figure

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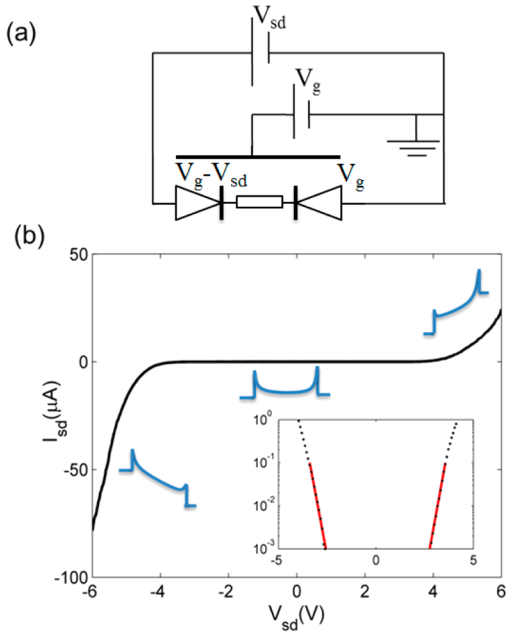

Figure 2. (a) Scheme of electrical circuit. The device is shown as back-to-back Schottky diodes. (b) $I-V$ characteristic at gate voltage $V_G = 0$ V. The inset band diagram shows the potential profile at different source/drain bias. (inset) Low-bias current onset plotted in semi-logarithmic scale. The straight line shows a fit by the model of thermionic emission with Schottky barrier height $\phi = 0.85$ eV.

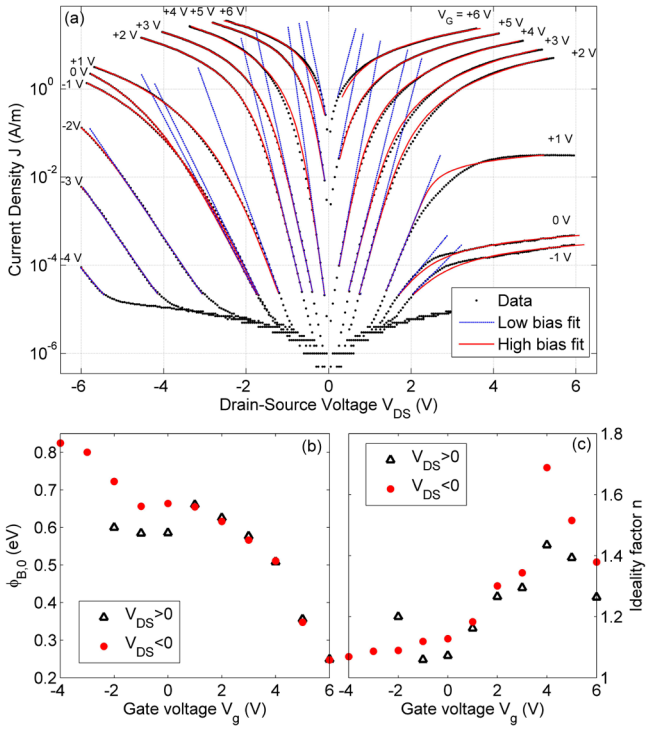

Figure 3. (a) Current−voltage ($I-V$) characteristics for gate voltage from $V_G = -4$ to +6 V, as labeled. Data (black points) are plotted in semilogarithmic scale and compared to the low-bias fit (blue dashed lines, backward biased Schottky junction) and to the high-bias fit (red solid lines, backward biased Schottky junction and space charge limited current in the 2D channel). (b) Schottky barrier height and (c) ideality factor were determined from low-bias data fit; two IV curves have been averaged for each increasing (black triangles) and decreasing (red points) gate voltage.

2b). As can be seen from Figure 2a, the DC power supply of the source/drain was common-grounded with the DC power supply for the top gate. This configuration causes asymmetrical $I-V$ characteristics as it produces a local gate voltage difference at each diode, i.e., one diode experienced a local gate voltage $V_g - V_{sd}$, while the other diode experienced a local gate voltage V_g. The symmetrical $I-V$ characteristics can be recovered by disconnecting the top gate (see Supporting Information for details) resulting in a floating gate.

The room temperature $I-V$ characteristics are shown in Figure 3a for top gate voltages from −4 to +6 V. The positive top gate bias switches the current on, which indicates n-type conductivity. At the gate voltage of +6 V and source/drain bias of −6 V, current density up to 35 A/m was observed. The graphene/SiC thermionic-tunneling junction is first described solely by thermionic emission of electrons over the edge Schottky barrier (junction of two coplanar conducting channels; graphene-to-SiC/Si_2O_3 interface). The minimal barrier height is expected to be located at the graphene-to-silicate edge, as shown by XPS band bending analysis. The MEG source and drain form an atomically thin interface with SiC; thus, the structure is essentially planar. The thermionic emission model for current between two coplanar contacts then reads[23]

$$I = A^* T^{3/2} W \exp\left(-\frac{q\phi_B^{\text{eff}}}{k_B T}\right) \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (1)$$

where W is the width of the conduction channel, q is the electron charge, k_B is the Boltzmann constant, T is temperature, V is the applied voltage, ϕ_B^{eff} is the effective barrier height at zero source/drain bias voltage, and n is the ideality factor. A^* is the two-dimensional (2D) effective Richardson constant $A^* = ((qM_c k_B^{3/2})/(\pi\hbar^2))(m_t/2\pi)^{1/2}$, where M_c is the number of equivalent conduction band minima in 6H-SiC,[24] $M_c = 6$, $\hbar$ is the reduced Planck constant, m_t is the effective mass in the 2DEG, which is the transversal mass for 6H-SiC, $m_t = 0.42\ m_0$, m_0 is the electron rest mass. The 2D-Richardson constant at $T = 300$ K is $A^* = 0.35$ A/m $K^{-3/2}$. The Schottky barrier transistor is composed of two Schottky diodes and a conduction channel, which satisfies the following relation $V = V_1 + V_2 + V_3$, where V is the total voltage drop between two multilayer graphene contacts, V_1 is the voltage drop on the reverse-biased diode, V_2 is the voltage drop on the forward-biased diode, and V_3 is the voltage drop in the rest of the channel. The channel resistance R_3 (associated with voltage drop V_3) can be estimated from the linear high bias $I-V$ characteristics to be $\sim 10^4$ Ω. Therefore, when the current in the channel is small ($I < 0.1$ μA), the voltage drop across the channel can be neglected. The total voltage drop is approximately written as $V = V_1 + V_2$. The blue dashed line in Figure 3a shows the low-current fit using Schottky barrier height ϕ_B^{eff} and ideality factor n as fitting parameters. Both fitting parameters as a function of top gate voltage are shown in Figure 3b,c, respectively. The barrier height spans 0.65−0.85 eV for different devices. The expected value of the edge Schottky barrier height can be estimated from XPS band bending analysis. The SiC/MEG band bending +0.7 eV and the position of the Fermi level $E_F = 0.8$ eV below the conduction band give a bulk-to-bulk planar barrier of 1.5 eV (Supporting Information). The SiC/silicate band bending −0.6 eV gives a

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bulk-to-bulk planar barrier of 0.2 eV (= 0.8−0.6 eV). Since the SiC is homogeneously doped, the depletion width should be even on both SiC/MEG and SiC/silicate side from the edge barrier, hence the edge barrier height is assumed to be (1.5 + 0.2)/2 = 0.85 eV. This is in agreement with experimentally obtained values. The barrier height is further lowered by 0.5 eV applying positive gate voltage, which is six times more than what is expected for the Schottky effect.[25,26] The high gate voltage sensitivity can be explained by the two-dimensional nature of fringing fields around source and drain contacts. On the basis of our finite element method calculations of electrostatic potential in the simplified device geometry (Supporting Information), the fringing fields are up to 2 orders of magnitude stronger than fields given by $E_{3D} = V_{ds}/L$, where V_{ds} is a drain-source bias and L is a channel length. Since the Schottky barrier lowering due to the Schottky effect scales as $E^{1/4}$, these fringing fields account for the factor of 3 in a discrepancy between data and the simple Schottky effect. The finite screening length in MEG will effectively thin the source and drain contacts, leading to even stronger fringing fields and stronger barrier height lowering. A variable Fermi energy in a top graphene layer seamlessly connected to the conduction channel[27] is also a source of barrier lowering.[12] We show below that, besides barrier lowering, the tunneling is another consequence of strong fields at source and drain.

At the high source/drain current, the voltage drop in a channel has to be taken into account ($V_3 \neq 0$). To determine the conduction mechanism, the power-law dependence for the channel conduction was assumed to be $V_3 = \alpha I^{1/\beta}$. With the effective barrier height and ideality factor obtained from the fitting result of low source/drain current region, the $I-V$ characteristics at high source/drain current region can be fitted by taking β = 1.2−2.0. The nonlinear current−voltage characteristics indicate contribution of both drift and space charge limited current in the channel. This is in agreement with a depletion width[26] at the graphene/SiC junction, which spans of $W_{depl} \approx$ 100−360 nm (applied bias 1 to 6 V; vanadium doping $N_V = 1 \times 10^{17}$ cm^{-3}) and determines the region of space charge limited (SCL) current.[28] The current in the rest of the channel is predominantly given by drift (long channel regime conduction). It is well-known that in lightly doped semiconductors and insulators, the SCL current leads to the Mott−Gurney law (square law $I-V$ characteristics).[29,30] Note that SCL currents have been observed in thin wires,[31] vacuum gaps,[32] and polymer thin films.[33] Depending on the blocking and injecting contact properties, film thickness, trap content, trap energy level, the carrier density distribution over the channel, or a combination of several transport mechanisms, the power law can deviate from 2.[34] Because of the combination of two transport mechanisms, the field effect mobility has been only estimated by assuming drift driven channel length to be $L_{drift} \approx$ 500 nm (= $L - W_{depl}$, where L is total channel length and W_{depl} is a depletion width), giving μ_{FET} = 10−20 cm^2 V^{-1} s^{-1}. This is roughly 1/3 of the mobility in bulk vanadium-doped ($N_V = 1 \times 10^{17}$ cm^{-3}) 6H-SiC.

The drain-source current versus gate voltage is plotted in Figure 4 for drain-source bias from −6 to +6 V. Data show strong bias dependence of the threshold voltage, see Figure 5a, which is a consequence of strong two-dimensional electrostatic fields at the source contact. Devices exhibit superior on/off ratio up to 5×10^6 and subthreshold swing 300 mV/decade, see Figures 4 and 5b.

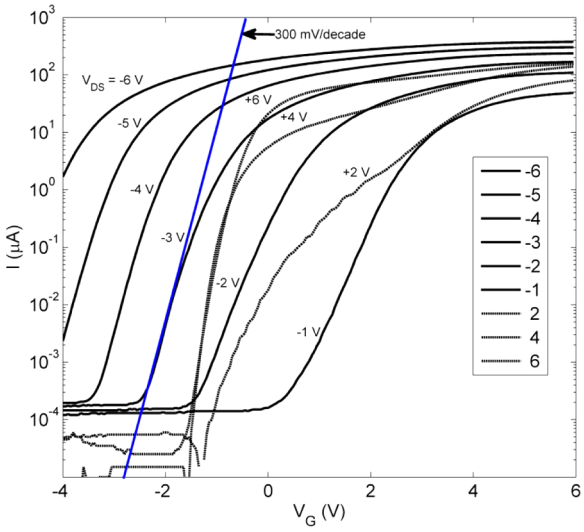

Figure 4. Drain-source current versus top-gate voltage for drain-source bias V_{DS} = −6, −5, −4, −3, −2, −1, +2, +4, and +6 V. The blue line depicts a slope of 300 mV/decade.

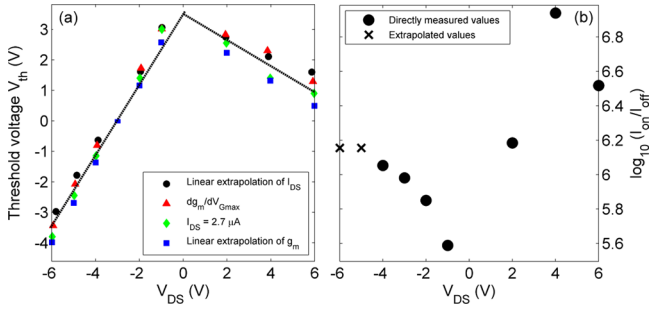

Figure 5. (a) Threshold voltage has been determined by linear extrapolation of drain-source current (black points), maximum in derivative of trans-conductance (red triangles), constant current method (green diamonds), and by linear extrapolation of trans-conductance (blue squares). (b) On/off ratio was determined from current versus gate voltage characteristics (Figure 3). The on/off ratio for $V_{DS} > -5$ V was determined directly from the data (black circles); on/off ratio for V_{DS} = −5 and −6 V was determined by linear extrapolation (black crosses) due to the lack of experimental data at $V_G < -4$ V.

The tunneling component to the overall device conduction is identified in the temperature dependence of current−voltage characteristics. The $I-V$ characteristic at zero gate voltage is shown in Figure 6a. The data has been fitted in the low-current regime giving ideality factor n = (1.10 ± 0.05), which is consistent with the value obtained at room temperature. The barrier height shows, however, a very strong temperature dependence that is not expected for purely thermionic emission over the Schottky barrier. This is a consequence of tunneling through a thin barrier induced by two-dimensional fringing fields at the source contact. Considering tunneling probability in Wentzel−Kramers−Brillouin (WKB) approximation and taking the low temperature barrier height ϕ_0 = 0.25 eV, an effective barrier thickness δ can be determined from the slope of the barrier height temperature dependence (Figure 6b), $\phi_{eff} = \phi_0 + \delta(\phi_0)^{1/2}((2(2M_C m_t)^{1/2})/\hbar)(k_B T/q)$ to be δ = 3.5 nm. Using a solely thermionic model implies an unphysically large, temperature-dependent barrier height. However, this discrepancy is resolved, assuming a significant tunneling component.

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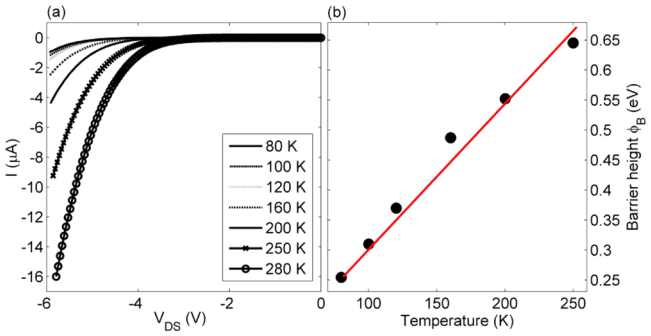

Figure 6. (a) Temperature dependence of drain-source current versus drain-source bias for T = 80, 100, 120, 160, 200, 250, and 280 K, measured at V_G = 0 V. (b) Barrier height as a function of temperature.

We note that δ is only an effective barrier thickness and that the actual barrier height and thickness strongly depend on external bias and top gate. Since the tunneling probability is an exponential function of ϕ and δ, also the threshold voltage then strongly depends on applied bias and top gate, as has been observed experimentally; see Figure 5a. The appropriate numerical modeling without former approximations requires self-consistent solution of Poisson equation and nonequilibrium quantum transport as has been done for example in the case of Schottky barrier carbon nanotube FETs.[35]

Besides the successful fabrication of thermionic emission-tunneling based field effect transistor, the issue of low channel mobility and relatively small subthreshold swing need yet to be addressed. The channel mobility is mainly limited by bulk mobility of highly vanadium-doped semi-insulating SiC and possibly by nonideal SiC/gate oxide interface. The former can be solved by using semi-insulating SiC wafer with lightly doped top epilayer.[36] Counter doping is known to reduce interface scattering.[37] Although the density of interface states is low enough to allow formation of the accumulation layer, it needs to be further reduced in order to lower subthreshold swing to the thermionic limit 60 mV/decade.[26] We note that, since the current is governed both by thermionic emission and tunneling in our devices, reducing the density of interface states D_{it} might presumably lower the subthreshold swing to subthermionic limit values.

In summary, a Schottky barrier transistor with multilayer epitaxial graphene contacts was fabricated, characterized, and analyzed. A two-dimensional electron gas was formed at the interface of SiC and ordered oxide Si_2O_3 after high temperature vacuum annealing. The crystallographic structure and surface electrostatic arrangement has been confirmed by LEED and XPS experiments, and the formation of the accumulation layer has been modeled by numerical calculations. Superior on/off ratio up to 5×10^6 has been achieved, subthreshold swing reaches 300 mV/decade, and the device can sustain large current densities up to 35 A/m. The estimated channel carrier mobility 10−20 $cm^2\ V^{-1}\ s^{-1}$ is believed to be limited by the highly vanadium-doped SiC substrate; hence, using a standard wafer with conducting (naturally doped) epilayer might increase this parameter toward commercially favorable values. Schottky barriers on the channel edge were observed to strongly depend on gate voltage and temperature. These effects were assigned to fringing two-dimensional electrostatic fields, which cause thinning of the barrier and induce parallel conduction channel in a form of temperature-independent tunneling. We have concluded that the barrier height in the solely thermionic emission model gains effective temperature dependence if tunneling is neglected.

■ ASSOCIATED CONTENT

Supporting Information

Full description of the device fabrication process, LEED data measured on a regraphitized device and detailed LEED data interpretation, band diagrams of SiC/MEG and SiC/Si_2O_3 interface based on XPS data, local density approximation (LDA) calculations of the interface eigenstates, finite element method (FEM) calculations of the electrostatic potential in the device, comments on an alternative explanation of the Schottky barrier height temperature dependence, origin of the asymmetry in current−voltage characteristics, and an example of the threshold voltage analysis. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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