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Controlled epitaxial graphene growth within removable amorphous carbon corrals

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We address the question of control of the silicon carbide (SiC) steps and terraces under epitaxial graphene on SiC and demonstrate amorphous carbon (aC) corrals as an ideal method to pin SiC surface steps. aC is compatible with graphene growth, structurally stable at high temperatures, and can be removed after graphene growth. For this, aC is first evaporated and patterned on SiC, then annealed in the graphene growth furnace. There at temperatures above 1200 °C, mobile SiC steps accumulate at the aC corral that provide effective step flow barriers. Aligned step free regions are thereby formed for subsequent graphene growth at temperatures above 1330 °C. Atomic force microscopy imaging supports the formation of step-free terraces on SiC with the step morphology aligned to the aC corrals. Raman spectroscopy indicates the presence of good graphene sheets on the step-free terraces. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4890499]

To be technologically viable, graphene must be grown in a well controlled manner. Beyond preparing well ordered 2-dimensional graphene films, growth needs to be tailored at the nanoscale to produce the desired devices at pre-defined locations. Epitaxial graphene on silicon carbide (EG on SiC) meets these criteria.[1] EG has excellent electronic transport properties, including record high frequency operation,[2] record spin diffusion lengths,[3] and room temperature ballistic transport.[4] Single layer nanoribbon growth has been produced on the SiC sidewalls of plasma etched steps[4,5] and EG thickness control was demonstrated on etched mesas.[6] Selective graphene growth was also achieved by capping flat SiC with a high temperature stable layer to prevent (or enhance) graphene formation.[7–9] Progress in graphene growth selectivity was shown using Chemical Vapor Deposited (CVD) methods, where an oxide barrier[10] provides better growth control on Cu and self-assembled nanoribbons on gold surfaces have been demonstrated.[11] Unlike CVD methods, however, the advantage of EG for technological development is to be scalable directly on a high quality semi-insulating substrate. Further advantages of EG include its integration with silicon[12] and SiC electronics.[13]

This Letter focuses on locally controlling the step bunching of SiC during EG growth. Although EG grows like an overlaying carpet on the stepped SiC surface, steps provide graphene nucleation sites on the Si face that need to be controlled.[6,14,15] Furthermore, underlying SiC steps induce slight additional electronic scattering in graphene.[16] Steps tend to bunch into unit cell high steps,[17] which is 1 nm high for 4H-SiC. Their spacing is determined by the local miscut angle, which for on-axis wafers is typically in the range of 0.1°–0.5°, giving step spacing of 600 nm–110 nm which will vary throughout the surface. Under the proper H_2 etching and growth conditions higher step heights give correspondingly wider terraces, often around 1 μm wide.[18] However, a naturally formed surface cannot have an arbitrarily determined step width, location, or orientation. This means that steps are likely to be located within a typical 1 μm wide randomly positioned graphene device.

To successfully tailor growth of EG on SiC requires placement of structures that anchor graphene growth templates and that are stable on the SiC surface at EG growth temperatures. Preparation of regularly spaced SiC steps by hydrogen etching can be preserved in a range of growth parameters[18] but generally leads to further step bunching at the graphene growth temperature ($T > 1300$ °C in the confinement controlled sublimation (CCS) method[19] or higher under Ar pressure[20]). These methods cannot provide a precise alignment of the steps. Precise alignment of steps was achieved at the edges of etched mesas in Refs. 6 and 19 or trenches[21] etched into SiC. However, this method requires a large mesa

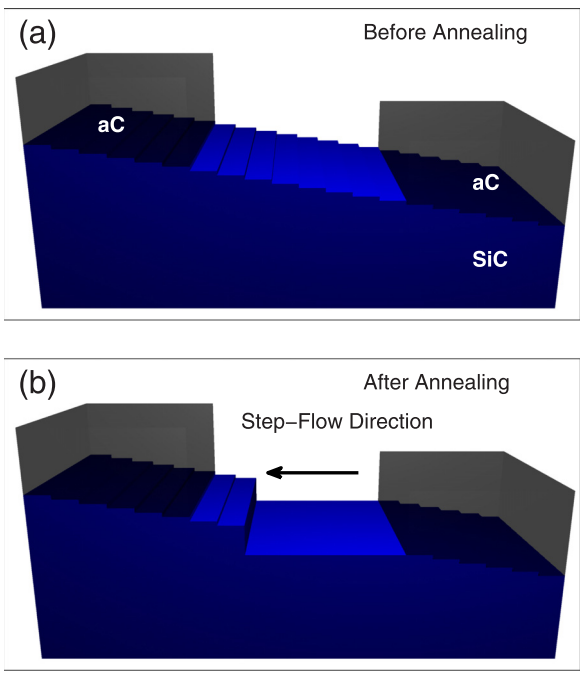

FIG. 1. aC step pinning process. Depicted in (a) are the SiC steps occurring before the graphene growth. In (b), the mobile steps have accumulated to the lower free energy configuration.

height to preserve the mesa during high temperature step flow. This is neither compatible with device production (metal interconnects for circuitry must cross the mesa step), SiC electronics,[13] or with integration to a silicon wafer by wafer bonding that requires flat surfaces.[12] A better method is necessary.

Any surface configuration that can prevent step flow on SiC will structure step bunching. Step flow control has similarly already been demonstrated on silicon.[22,23] Deeply etched grid features in these silicon samples enclose the step-flow[22,23] and align the steps to grid features after step-flow occurred.

The principle of step-flow control is to harness the surface free energy minimization such that step bunching is favored at one end of the enclosure. As previously demonstrated, step-flow on Si is mediated by evaporation of the Si atoms from the surface.[22,23] However for SiC, step-flow can occur prior to and during epitaxial graphene growth.[15] If graphene is growing, step flow due to Si sublimation is possible, but unlike in silicon, the step flow on SiC before EG growth conserves mass.

Recognizing that graphene layers hinder step-flow,[19] and that graphitic materials are also high temperature stable, we propose here to enclose the naturally occurring surface steps on SiC with evaporated amorphous carbon (aC). Compared with other refractory materials, amorphous carbon is completely compatible with graphene growth as it will not introduce additional chemical elements. Annealed aC forms nanocrystalline graphite[24] and is at least as structurally stable as graphene, such that it retains its patterned shape after growth. Another important advantage of aC is that it is removable with oxygen plasma after growth, so that it is compatible with processes requiring flat surfaces such as silicon wafer bonding or Si (Ref. 12) and SiC electronics.[13] This is unlike mesa structures for step flow control, which cannot be removed after growth. See Figure 1 for a schematic cutaway of the step bunching controlled growth.

We prepared EG samples using nominally on-axis 4H SiC (0001) and $(000\bar{1})$ substrates cut to 3.5×4.5 mm^2. The actual miscut angle is up to 0.1°. The samples were ultrasonically cleaned for 30 min each in acetone and isopropyl alcohol. Three samples were studied: G1, which has monolayer graphene grown on the hydrogen etched Si-face, G2 which is

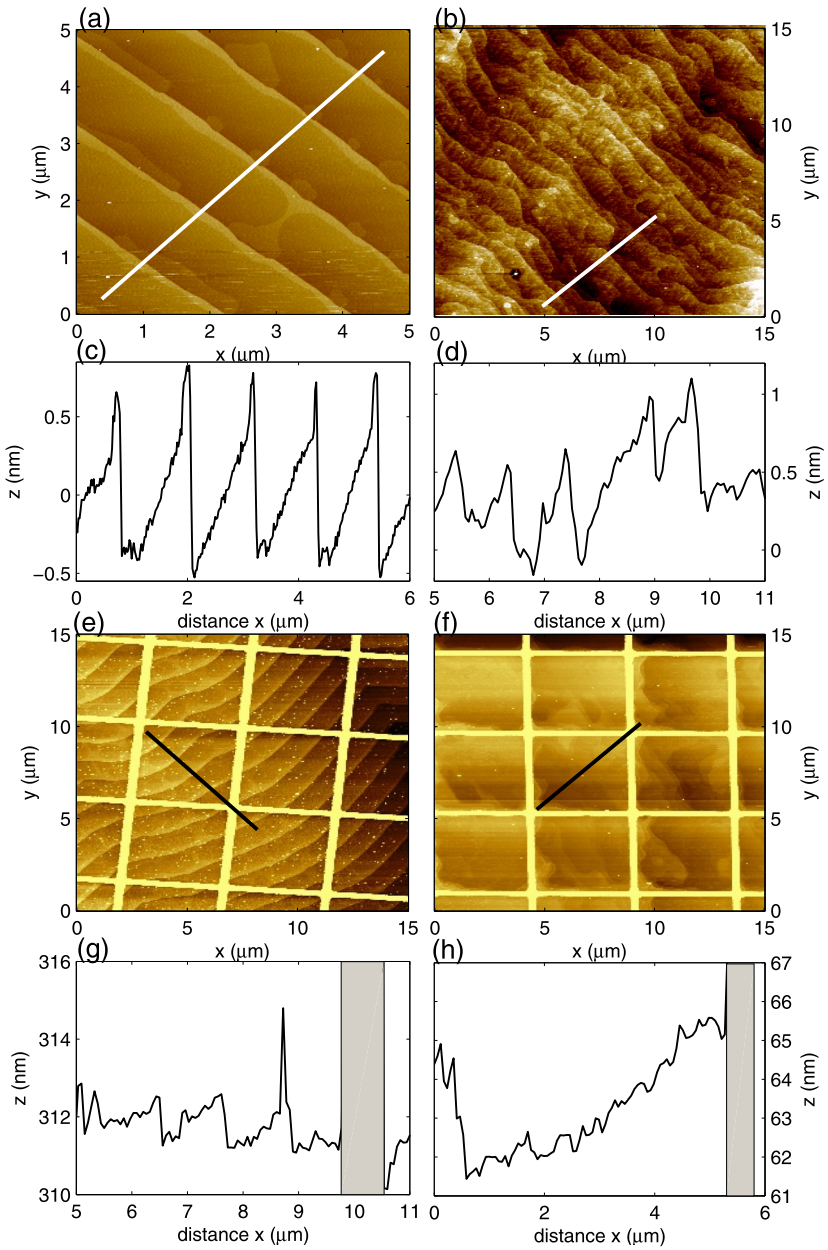

FIG. 2. AFM images of the surface of hydrogen etched SiC(0001) (a) before and (b) after graphene growth. The corresponding step profiles taken along the step flow (white line in (a) and (b)). AFM topographic image (e) before and (f) after graphene growth using the amorphous carbon grid and corresponding profiles along step flow (g) and (h), respectively.

multilayer graphene grown on the polished C-face,[25] and B1 which is buffer layer grown on chemical and mechanically polished Si-face. Sample G1 was hydrogen etched in a 40 cc/s (3% H_2)/(97% Ar) flowing forming gas mixture at 1450 °C at 1 atm. The hydrogen etched surface has well defined SiC steps before the step controlled graphene growth. As seen from Figure 2, the initial step height on the hydrogen etched sample is 1 nm, corresponding to one SiC unit cell.

aC is deposited using a Cressington 108A carbon deposition system modified for high vacuum use. Deposition occurs by resistively heating a graphite rod point contact junction to a temperature exceeding the temperature of graphite sublimation. A 3 Ω junction evaporates at 120 A. The aC was uniformly deposited at 10^{-6} mbar over the entire sample. A typical thickness of 20 nm is deposited.

The aC is then patterned into a $5 \times 5\ \mu m^2$ square grid pattern using standard e-beam lithography and etched away using an oxygen plasma. Once the aC is etched through, any overetch into the SiC will introduce a silicon oxide passivation layer to the SiC, which is maximally a few nanometers thick. The oxide thickness is self-limiting.

The samples are cleaned overnight in acetone to dissolve the remaining resist, and then the samples are rinsed with isopropyl alcohol. Graphene samples are grown using CCS in a graphite enclosure in an induction heated furnace.[19] The sample is annealed at 1150 °C for 20 min to remove silicon dioxide,

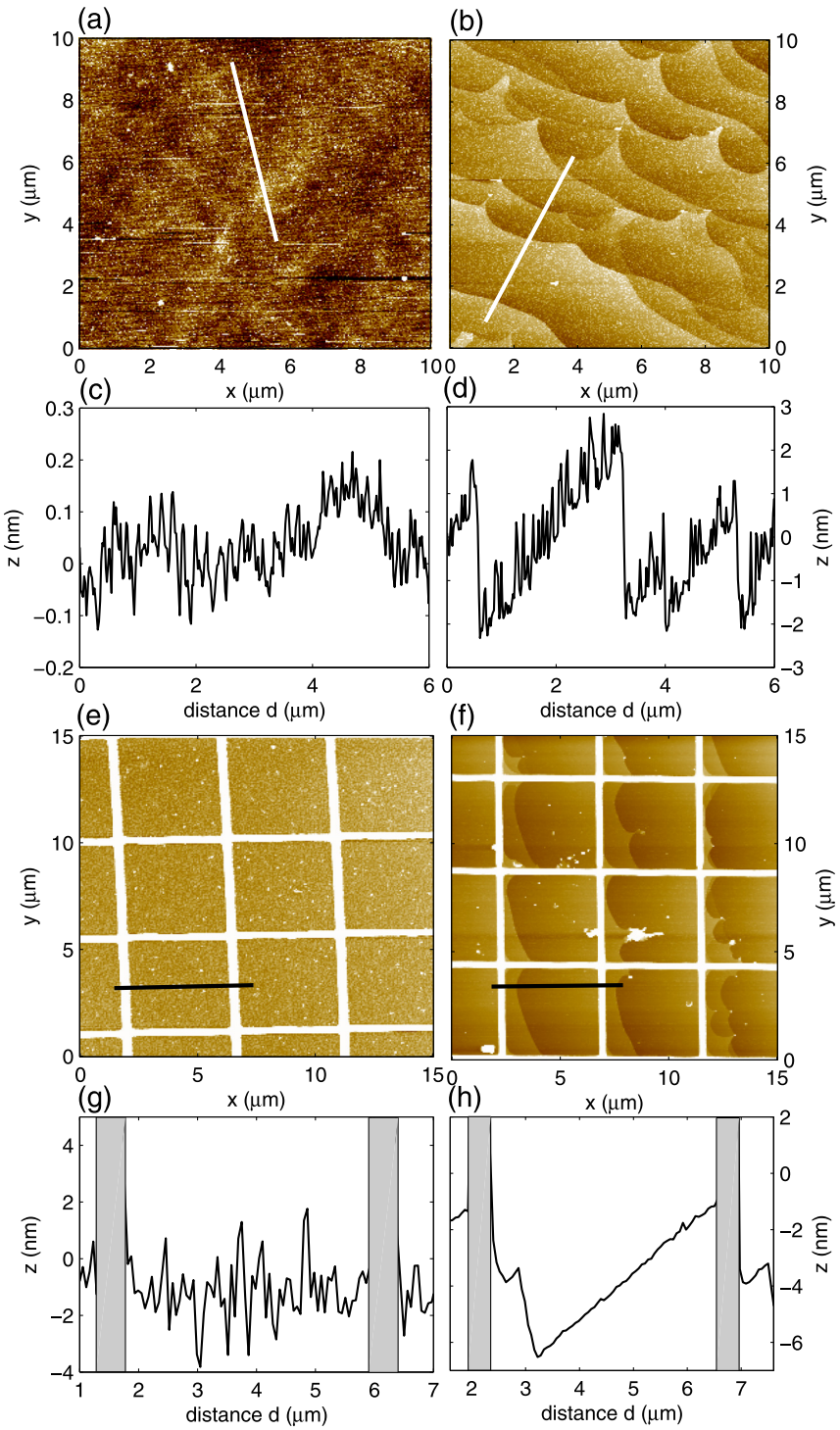

FIG. 3. As in Fig. 2 but here for sample B1. The SiC surface was chemically and mechanically etched prior to growth. The process of buffer formation without aC grid (a) before and (b) after buffer growth, corresponding profiles (c) and (d). The surface morphology using aC grid (g) before and (h) after buffer growth. Corresponding step profiles along the step flow are shown in figures (g) before and (h) after buffer growth.

and then the graphene growth step proceeds. The Si-face graphene sample G1 was grown at 1600 °C for 40 min and the buffer layer sample B1 was grown at 1350 °C for 30 min.

Characterization of the surface topography at various stages of process was done using non-contact mode atomic force microscopy (AFM). Before the growth on the unetched surface, there is a nanometer scale roughness in the region within the aC enclosure.(Figure 3(e)) The surface becomes smoother after the graphene growth due to removal of the surface oxide layer. On Figure 2(e) and 2(f) note that the orientation of the steps is different in each sub figure. This is due to differing local wafer miscut throughout the sample surface.

See Figures 2(f) and 3(f) for the AFM topography after the sample growth. The step morphology aligns to the aC grid on all samples. The 0.5 nm scale roughness seen in Figure 2(f) is due to contamination on top of the graphene after the graphene growth. Larger, nanometer sized aC particles from the aC deposition pin the steps seen in sample B1 away from the gridded area into a pinched shape (Figure 3(b)). Nanometer sized aC particles are deposited in greater numbers as the carbon rod source is heated to higher temperatures.

An important feature to note is that the aC grid remains stable throughout the graphene growth process. Comparing the width and size, as well as height (20 nm) of the aC features in Figures 2 and 3 before and after growth yields no differences to within a nanometer. Furthermore, the original SiC step features are seen underneath the aC. See, for example, the SiC steps that remain under the aC in supplementary Figure S1 (Ref. 25) on the C-face. This means the aC is structurally more stable than the SiC surface it rests upon, and is providing the barrier to SiC step movement.

Before growth the typical step width on sample G1 (Figure 2) is 0.96 μm. After growth away from the grid the typical step width is 0.22 μm, and within the grid the step width is increased to 1.9 μm. On sample B1 (Figure 3), the typical step width before growth is 0.2 μm. After growth, the typical step width away from the grid is 1.4 μm and within the corral the step width is 3.3 μm. In both hydrogen etched (G1) and non-hydrogen etched (B1) cases, the presence of the step flow barrier increases the typical step width. In comparison, steps pinned by mesa edges on the Si-face yield step-free terraces up to 1 μm,[6] whereas the use of the aC corral provides comparable if not larger step-free areas by using favorable growth conditions. Similar results are observed on sample G2.[25]

Figure 4 shows Raman spectra for samples G1 and B1. The Raman laser spot was focused on the aC grid in Figure 4(a), and within the aC grid, for samples G1 and B1 in Figures 4(b) and 4(c), respectively. Using Non-negative Matrix Factorization (NMF) spectral decomposition, the Raman spectra were separated into their principle components.[26] In each case, two principal components are found, representing either the aC, graphene, and buffer layer, respectively, with SiC underneath. Notably, no graphene component is found for Figure 4(a), confirming that the aC effectively caps the SiC to prevent graphene growth. The Raman component that corresponds to the aC indicates nanocrystalline graphite. The ratio of the D to G peak intensity $\frac{I_D}{I_G} = 0.86$ corresponds to a graphitic crystallite size of 20 nm.[27] This is expected since nanocrystals form upon annealing the aC at graphene growth temperatures. For the spectrum in Figure 4(b) of sample G1, the graphene

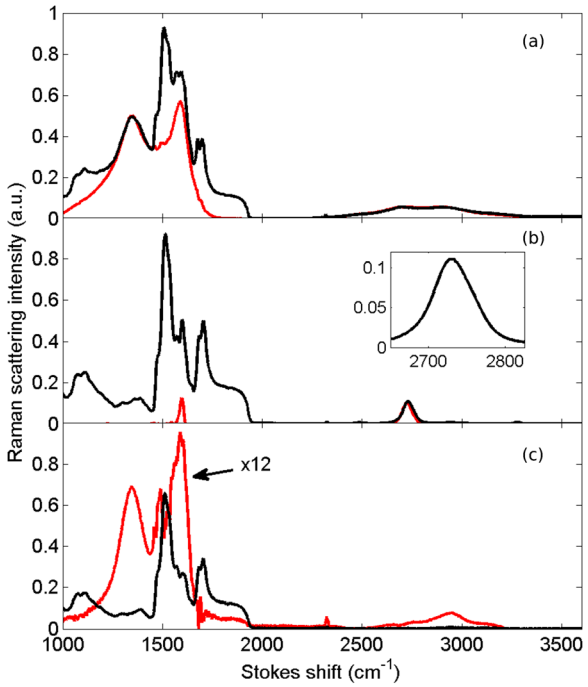

FIG. 4. Raman scattering spectra (using a $\lambda = 532$ nm laser) with the laser spot focused on: (a) the aC grid. In black: aC and SiC; in red: aC from NMF spectral decomposition. (b) Sample G1 within the aC grid. In black: graphene and SiC; in red: bilayer graphene NMF component; inset: graphene 2D peak. (c) Sample B1 within the aC grid. In black: SiC and buffer; in red: buffer layer.

component, which has not had the much weaker buffer layer Raman component separated, shows no D peak at 1350 cm^{-1}, indicating excellent structural order. The 2D peak centered at 2730 cm^{-1} has a FWHM of 63 cm^{-1}. This width is consistent with Si-face bilayer.[28] The buffer layer Raman component in Figure 4(c) for sample B1 has a much weaker signal than graphene and is similar to previously published buffer layer spectra.[29,30] In both G1 and B1 cases, Raman spectra show that good graphene or buffer were grown with aC nearby.

Finally, we remove the aC corral to demonstrate electrical contact to a corralled area. aC is first evaporated on SiC and patterned in the same step in the shape of corrals, as above, and leads for electrical probing. A buffer layer sample is then grown. After growth the aC corral structure is selectively removed using an oxygen plasma through a patterned mask. aC is totally removed at some places while kept in other areas to serve as electrical leads to graphene. This is seen in the AFM image in Figure 5. The shape of removed corral features are still visible in the AFM. The 2 nm step height between the removed corral and the growth region is due to silicon dioxide formed by the previous oxygen plasma etch but was removed during growth. The roughness of the Hall bar shaped region is due to resist residues. As for aC used as electrical leads, annealed amorphous carbon has a conductivity approaching that of graphite.[24] aC contacts made in the portion of the corral with bunched steps may not be as desirable, due to transport being over a step. aC also can be used to improve graphene performance by having a clean surface after growth with no resist residues, which has already been demonstrated to improve device performance.[31] In the present example, the aC contacts are provided to a buffer layer that is not conducting. Because after the final etch there is no aC Raman signal, and because there is no ohmic contact

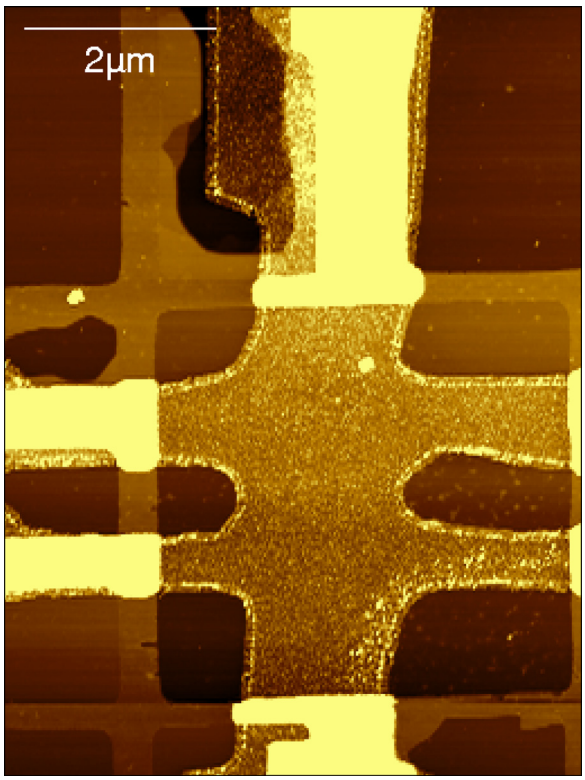

FIG. 5. Buffer layer sample grown on single terrace SiC by the aC corral method. Central region: H-shaped Hall bar (roughness is due to resist residues) provided with aC leads (white) that have been evaporated and patterned together with the aC corral and prior to buffer layer growth. The rest of the aC corral (light grey grid) has been removed in the same etching step that defined the Hall bar.

between the aC leads, we conclude that the aC corral was completely removed while preserving the step-free region.

Further step-flow experiments include modifying the aC grid, the wafer miscut, and the growth conditions. Different aC step flow enclosures will tailor the step orientation according to the boundary conditions set by the grid. Additionally, an insulating alternative to aC, like oxides or diamond-like carbon, may be complementary to the conductive aC. Performing step flow control on vicinal cut wafers may yield more reproducible step bunching, since the total miscut angle will not be as sensitive to the miscut angle uncertainty. The step bunching is likely to be greater as well on vicinal cut wafers, thereby enhancing the step flow control.[17] Finally, by increasing the gas pressure in the CCS furnace it is possible to raise the onset temperature of graphene growth.[19] This would increase the step flow rates to possibly reach lower surface free energy before graphene forms and therefore inhibits step-flow during graphitization.

In conclusion, we have shown that evaporated amorphous carbon is effective for structured EG growth and is completely compatible with the CCS growth method. We have demonstrated that SiC step bunching is pinned by an aC cap that acts as a step flow barrier. The patterned aC grid is structurally stable on an active SiC surface and the step morphology is aligned to the aC grid. Good single layer graphene is grown on up to 4 μm wide step-free areas which locations are predefined by lithography. Lastly, we demonstrate that the great advantage of aC corrals is that they are selectively completely removable after growth for planar process compatibility, and the recrystallized aC, evaporated prior to graphene growth, can also be used as electrical leads.

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