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ABSTRACT

Pulse delay generators are ubiquitous in laboratories to coordinate and control the timing between different devices in applications that include lasers, mass spectrometers, and other scientific instruments. The most important required characteristics are precision, to control time exactly, and low-jitter, to minimize uncertainty in experiments. Here, we introduce a new design of a high precision and low-jitter digital delay generator based on a Field Programmable Gate Array (FPGA). The final delay is composed of steps of 4.2 ns (coarse delay) with fine steps of 16 ps (fine delay). The coarse delay is generated by a 240 MHz pulse sequence from the FPGA with a 50 MHz clock. An embedded time-to-digital conversion unit is used to measure the interval between the external trigger and the clock signal, which, together with an integrated delay generator, is used to realize the fine delay. Jitter compensation is achieved through a measurement-and-feedback module. A computer interface is designed to control the system through a Nios II processor. Measurements confirm a time resolution of 16 ± 2 ps with jitter below 450 ± 20 ps (at 24 °C) with a maximum delay of 1 s. The whole system is simple in structure and low in cost.

I. INTRODUCTION

A digital delay generator (DDG) is a device used to tune the timing between different devices or events, which is widely used in laser systems,[1,2] radar echo signal simulating systems,[3,4] Positron Emission Tomography (PET),[5] Automatic Test Equipment (ATE),[6] time-of-flight mass spectrometers,[7–9] and other wide spectra of scientific instruments.

The operational principle of a DDG is when an external signal triggers the device, an output signal is generated after a digitally set delay. It has been intensively explored in the past several decades, reaching sub-picosecond resolution and jitter.[6,10–13] One recently reported architecture, based on the subset sum delay line (SSDL), achieved a delay accuracy of 76 ps and a dynamic range of 32 ns.[14] Another design, based on the carry chain of Stratix III Field Programmable Gate Array (FPGA), demonstrated a device with a delay accuracy of 38.6 ps.[15] However, with the development of modern experimental requirements, there is urge of a DDG with even higher resolution of picosecond scale, larger time span of seconds, having multiple channels, low cost, and low jitter.[6] The common ways to realize this are the counter method[16] and the delay chip method.[17] The counter method can provide a wide time range, but its accuracy is limited by the sampling rate, while the delay chip method offers much higher precision; however, it has a far limited range. Aiming for those aforementioned needs, taking advantage of both technologies, the design presented here achieves several tens of picosecond resolution, 1 s of delay range, and more than ten full channels at extremely low cost.

II. DESIGN

The FPGA chip used here is the EP4CE6E22C8. It has an embedded time-to-digital conversion (TDC) module, two pulse generators, and a Nios II processor with the function of jitter compensation as shown inside the dashed-dotted line in Fig. 1. The total time delay of the DDG is composed of a coarse delay and a fine delay. The coarse delay is realized by using the counter method whose resolution is determined by the sampling rate. The 240 MHz clock signal is generated by multiplication of an external 50 MHz from a crystal oscillator, which is the maximum frequency that the system can run. To generate the fine delay, the coarse delay step is subdivided by the 8-bit control word of the integrated delay generator AD9501, giving a resolution of 4.2 ns/255 = 16.5 ps.[18] The block diagram of the system is shown in Fig. 1.

After the external trigger enters the system, it splits into two channels: the coarse delay is realized by one channel and the jitter is measured in the other by the TDC. The TDC measures the interval between the trigger and the clock signal and then outputs to the delay compensation module. Through the software interface, the personal computer (PC) sends the user delay setting to a Nios II processor, which will be allotted into coarse delay and fine delay and implemented via a CP2102[24] serial port bridge chip. The processor sends the delay information to the jitter compensation module through the parallel input output (PIO) IP core, which is responsible for processing the delay setting and the measured interval, and further yields the compensated delay consisting of coarse delay and fine delay. The compensated coarse delay will be directly sent to its corresponding module, while the compensated fine delay value is converted into 8 bits, and sent to the AD9501 to synthesize the fine delay. Finally, the delayed signal is output by the AD9501 chip.

The AD9501 works by comparing the output voltage of a ramp generator against a set DAC value, when they are equal, the delay pulse will be created. Initially, the ramping voltage is set to 0 (reset) by pulling up pin 4. Therefore, the coarse delay module outputs two pulses to the AD9501: one for triggering the fine delay and the other for resetting the ramp generator. The interval setting between these two pulses controls the width of the delay signal. The timing diagram of the module is shown in Fig. 2.

The highest delay resolution in the counter method is determined by the sampling clock frequency. In this design, the 240 MHz clock yields 4.2 ns unit of coarse delay. The time interval between the external trigger and the sampling clock (see Fig. 2) is randomly distributed from 0 to 1 clock period, which would lead to a jitter of 4.2 ns if no compensation was applied.

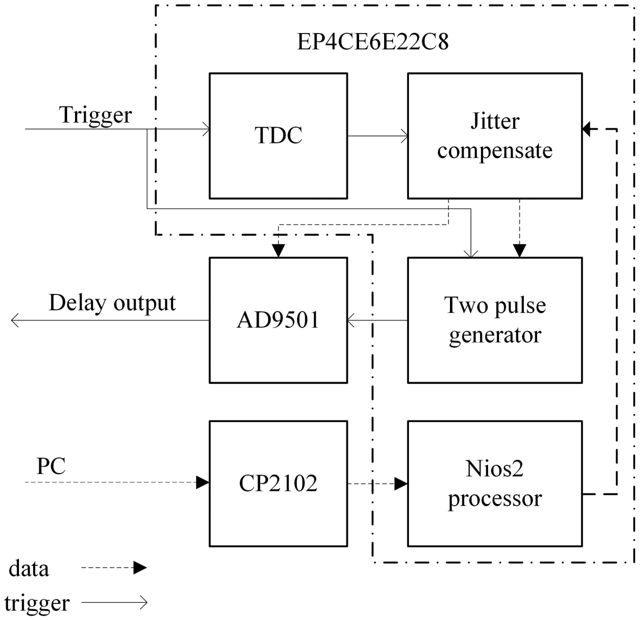

FIG. 1. Diagram of the system architecture. The solid line represents the trigger signal path, and the dotted line represents the data path. Function blocks inside the dotted-dashed line are the parts of FPGA chip.

The jitter measurement and compensation module measures the time interval between the trigger and the rising edge of the next clock signal and eliminates the jitter in the output signal. The most commonly used technique for time interval measurement includes current integration,[19–21] counter,[22,23] and time interpolation methods. This last method is realized by inserting much shorter time delay units into the interval and then counting the number of these units until it fills up the full span of the interval. This can be easily implemented in a FPGA and practically not only can improve system integration but also can reduce its cost. The construction of an interpolation circuit is realized simply by using the adder carry chain inside the FPGA[26–30] shown in Fig. 3.

The adder has two n-bit inputs. One is set to all 1 s, while the other has all the high (n − 1) bits at 0, leaving only the lowest bit for the external trigger signal. When the external trigger signal changes to 1, the addition operation is conducted from the lowest significant digit up. Because the lowest adder has its two inputs at 1, a carrier is generated and transferred to the next arithmetic unit for operation, where the inputs are 0 and 1, and a carrier is generated again, and so on. Hence, the pulse signal is transferred upwards in the add carry chain. When the clock signal arrives, the latch of the arithmetic unit locks the result of the adder. A value of 0 in an arithmetic unit indicates that the carrier was generated, and conversely, a value of 1 indicates that the signal did not reach that unit yet. Therefore, the latch locks a column of binary numbers "0000111111," where the position of the 0–1 jump indicates the location of the transmitted signal. Since the time span of each carrier unit is known, the number of zeros in the binary column can be converted to time, which realizes the measurement of the interval between the trigger signal and the clock signal.[31]

The interval measured by the carry-chain needs to be compensated in the total delay by subtracting it from the set delay. First, the delay will be separated into two parts: one is the maximum integer number of coarse delay units that can be fitted in the interval and the other is the reminder, which is less than a coarse delay unit. These two parts are called coarse delay part and the fine delay part, respectively. The realization of the coarse delay is by using the counter method, which is the integer number of fixed unit time of 4.2 ns, as mentioned above; the fine delay is realized by controlling an AD9501 chip through its 8-bit control word and reaches a resolution of 4.2 ns/255. The average length of each arithmetic unit is 0.073 ns,[25] so the time precision of the AD9501 is better than the carry-chain unit. For example, if the measured interval is 0.073 ns, 0.073 ns/0.016 ns ≈ 5, so we can compensate the 0.073 ns with 5 units of fine delay that express that interval. After analyzing the delay requirements, the operation is as follows:

(1) When the coarse delay is set to 0, only the carry-chain would be used to compensate the coarse delay jitter. The pulse delay will only come from the AD9501 with its fine delay.

(2) When the coarse delay is nonzero, the coarse delay counter kicks-in. The carry-chain will measure the interval between trigger and clock signal, and there would be the following cases:

   (i) If the measured interval "jitter" is less than or equal to the fine delay part, then the output coarse delay part will

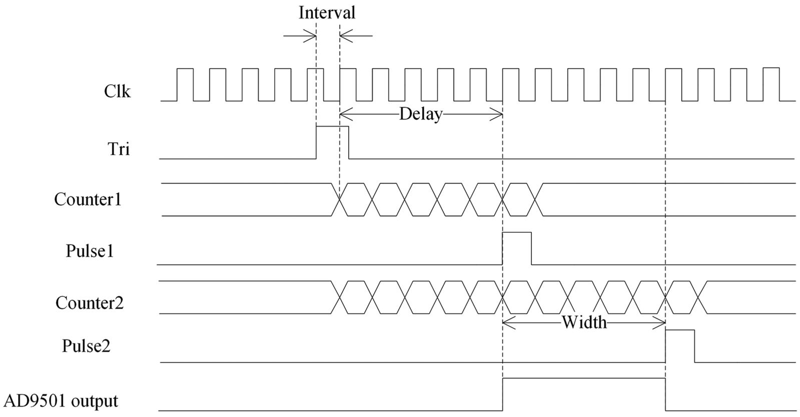

FIG. 2. Timing diagram of the coarse delay module. After the trigger signal arrives, the rising edge of the clock starts Counter1 and Counter2. When the counted value reaches the preset value of Delay, Pulse1 outputs a pulse. When the counted value reaches the preset value of Width, Pulse2 will output a pulse. Pulse1 acts on AD9501 to generate the rising edge of the delay output, and Pulse2 acts on AD9501 to generate the falling edge of the delay output.

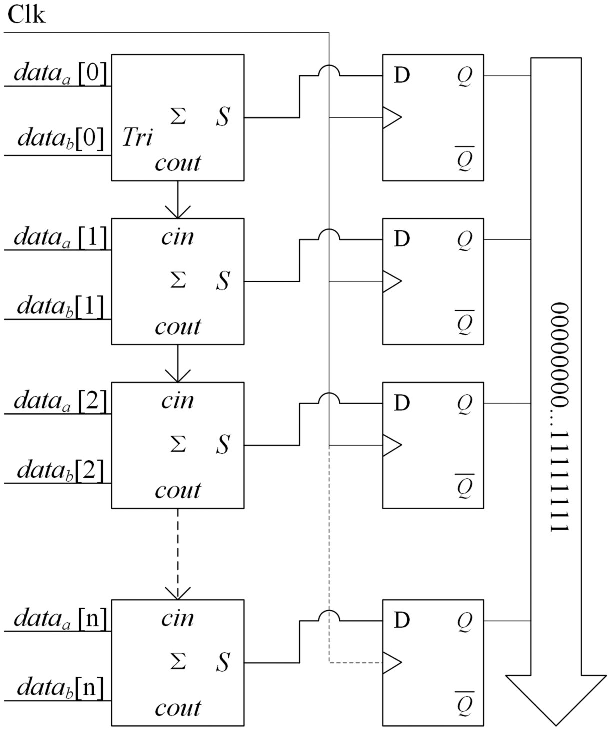

FIG. 3. Diagram of the interval measurement circuit. All the *data*$_a$ inputs are set to 1 and all *data*$_b$ to 0, except for *data*$_b$[0], which is connected to the trigger. When the trigger signal (*Tri*) arrives, the adder starts to operate from the least significant digit, outputs the result *S*, and generates the carry out *cout*, which is transmitted to the next carry input *cin*. The next arithmetic unit adds *data*$_a$ [1], *data*$_b$ [1], and *cin*, then outputs the result *S*, and generates its own *cout*. This way *Tri* propagates in the carry chain. When the clock rising edge arrives, the result of the arithmetic unit is locked by the latch, and the position reached by *Tri* is recorded in the form of a column of binary numbers.

stay the same, but the fine delay part will be compensated by directly subtracting the "jitter" from the fine delay part.

(ii) If the measured interval "jitter" is greater than the fine delay part, then one coarse delay unit (4.2 ns) will be moved to the fine delay part for subtraction. Since one unit of coarse delay represents 255 units of fine delay, the final output fine delay will be 255 units of fine delay added to the original fine delay minus the "jitter."

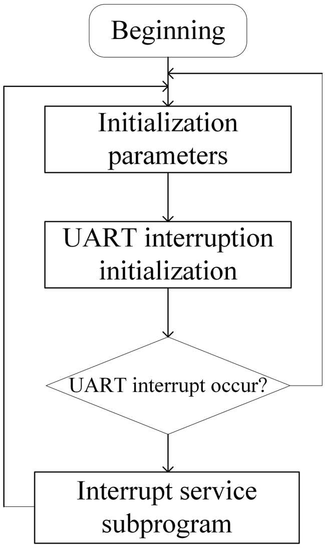
Beginning
Initialization parameters
UART interruption initialization
UART interrupt occur?
Interrupt service subprogram

FIG. 4. Flow chart of the control module. When the serial port receives the data from the PC, it triggers the UART interrupt and enters the processing function, which passes the PC data to each module through PIO.

Considering both the cost and the simplicity of the system, a Nios II soft core processor was selected. The processor receives the delay set by users from the PC, which then will be sent to the delay module. The performance can be further improved by using the IP core of Qsys. The IP cores that need to be added for data intaking and transmission are Universal Asynchronous Receiver/Transmitter (UART) and PIO. The PC sends the data to the read-register of the UART IP core through CP2102, the rxdata-register of the UART IP core receives the data, enables the read interruption, and assigns the read data to PIO, thus realizing PC's control over the delay system. Figure 4 shows the flow chart of the control module.

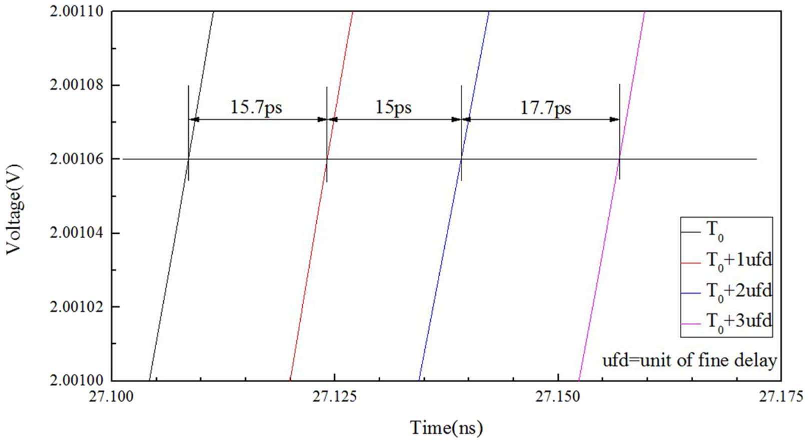

FIG. 5. Results of the highest resolution test. From these results, the measured resolution is better than 20 ps and is about 16 ps in average.

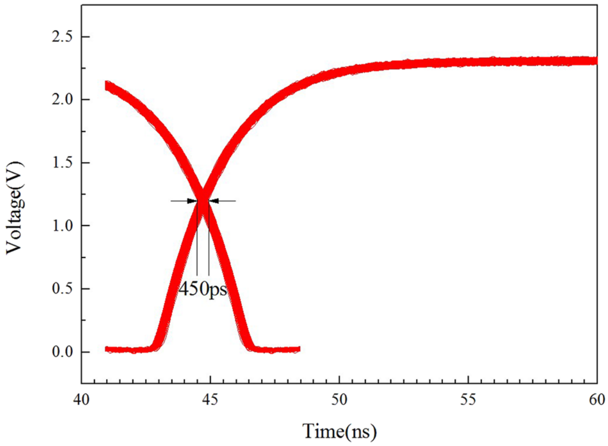

FIG. 6. Results of jitter measurements show that it is about 450 ps.

III. TEST OF PULSE GENERATOR

To measure the resolution of the DDG, a signal is generated by a DG535 (Stanford Research Systems) and connected to the input of the DDG and also to one channel of an oscilloscope serving as a trigger. Then, the output of the DDG is connected to another channel of the same oscilloscope for measuring. To measure the minimum delay of the output pulse, the oscilloscope display was set to average 4096 shots. Figure 5 shows an example of 3 tests, where 6 units of coarse delay and 126 units of fine delay are set as the reference T_0 with extra 1–3 units of fine time delay. The results of this test indicated that the resolution of DDG is on the order of 16 ps.

In order to measure the jitter, 500 shots were collected in the oscilloscope with fluorescence mode and are presented in Fig. 6. This gives an estimated jitter of 450 ps with the eye figure test, as shown in Fig. 6.

To test the stability of this device, the temperature dependent jitter and resolution measurements have also been conducted, which shows a marginal dependence as 18 ps delay resolution and 458 ps jitter at 53 °C compared to the ones shown above at 24 °C.

IV. CONCLUSIONS

This paper presents a new design of a FPGA based low cost delay pulse generator. It seamlessly combines the counter method to generate a coarse delay and an AD9501 for the fine delay, realizing high precision and wide dynamic range with 16 ± 2 ps timing resolution and 450 ± 20 ps jitter. The FPGA adder carry-chain is used to measure the time interval between the external trigger and the sampling clock and effectively reduce the jitter in the final pulse output. The resolution can be further improved by using newer chips with better performance. It can be easily used for a variety of scientific instruments for timing control with very low cost, rather high precision in a compact design.

ACKNOWLEDGMENTS

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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