

La-doped BiFeO₃ junction based random access multilevel nonvolatile memory

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ABSTRACT

Resistive switching devices are promising candidates for the next generation nonvolatile memories due to their outstanding performance, simplicity, and scalability. Among them, developing multilevel resistive switching has attracted great attention for its potential in significantly improving information storage density but without extra energy consumption. Although continuous multilevel resistive switching (CMRS) has been observed in many metal oxides and organic materials, achieving random access multilevel nonvolatile memories (RAMNM) with high speed and reliability is still pressingly needed for practical applications. Here, we have successfully fabricated a RAMNM based on high-performance pulse-width modulated memristive ferroelectric tunnel junctions (FTJs) of Pt/La_{0.1}Bi_{0.9}FeO₃/Nb:SrTiO₃ with giant switching ratios above 4×10^5 at room temperature.

1. Introduction

With the rapid development of technology such as 5G, AI (artificial intelligence), data mining, and self-driven vehicles, the demands for high density and speed, and low energy consumption of memory devices are greatly increased. In the past decades, minimizing their unit size has been the main theme of densifying storage capacity. However, high-density integration and low heat dissipation are two sides of the same coin [1]. Moreover, the higher device density will also inevitably raise the manufacturing challenge. An upfront solution will be magnifying the data storage in each memory unit instead [2–13]. As a possible solution nonvolatile resistive switching (RS) has been extensively studied in the past decade [14].

Unlike the conventional switching between two discrete states, the resistance in multilevel resistive states can be stored and read by the modulation voltage based on its hysteresis [12]. However, if the modulation sequence is fuzzed, multilevel resistance states may become indistinguishable [15]. Previous studies showed multilevel resistance states that can only be obtained by a fixed sequence of modulation, which is so-called CMRS [4,9]. In such devices, the storage unit must be reset through multiple writing operations each time when new data is written. It severely limits their applications [3,7,8]. The realization of RAMNM could become a complement of random-access memory (RAM)

for the next-generation of data storage devices. Therefore, obtaining the high stability of multilevel resistive states under fuzzed modulation is a challenge that has attracted much attention [12,13].

Ferroelectric tunnel junctions (FTJs) are fabricated by sandwiching an ultrathin ferroelectric layer between two electrodes, and the tunneling through the interfacial barrier is governed by ferroelectric polarization reversal [16]. FTJs have provoked extensive research interests in the last decade due to their simple structure, high switching speed and ratio, low energy consumption, long durability, and outstanding scalability [17–25]. In 2013, a metal/ferroelectric/semiconductor type FTJ of Pt/BaTiO₃ (BTO)/Nb:SrTiO₃ (NSTO) achieved a large switching ratio above 10^4 [16]. The ferroelectric polarization can modulate both its barrier height and width, which can be realized by simply applying different voltage pulses [22]. Similarly, BiFeO₃ (BFO) ultrathin film has also been used as a ferroelectric tunneling barrier obtaining a large switching ratio above 10^4 in super-tetragonal BFO based FTJs with high reproducibility (4×10^6 cycles). It has superior resistance contrasts than that in FTJs of Co/BFO/Ca_{0.96}Ce_{0.04}MnO₃ (CCMO) devices [26,27]. Later, a giant switching ratio up to 10^5 was reported with Sm_{0.1}Bi_{0.9}FeO₃ and La_{0.1}Bi_{0.9}FeO₃ (LBFO) [28,29]. They demonstrate the great potential of BFO and LBFO thin films for FTJ devices [30–42]. Although there are already a few reports about using FTJs to realize high-performance multilevel memory, the continuous

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electric modulation on the interfacial barrier is indispensable [23,28].

In this work, a random access multilevel non-volatile memory has been successfully fabricated with high-performance memristive Pt/LBFO/NSTO FTJ through magnetron sputtering. The distinct multilevel nonvolatile resistive states are generated using short voltage pulses with set widths. A tentative explanation of the mechanism is proposed based on the interfacial charge coupling, ferroelectric polarization reversal, and charge trapping/release by the external electric field.

2. Experiments and characterizations

Epitaxial LBFO thin films were grown on (001) single-crystalline NSTO (0.5 wt% Nb) substrates using radio-frequency magnetron sputtering (RFMS) deposition with a $\text{La}_{0.1}\text{Bi}_{1.0}\text{FeO}_3$ target. The temperature, pressure, and Ar/O₂ ratio were 650 °C, 0.7 Pa, and 50/1.8. For measurements, Pt top electrodes (30 nm thick, 100 or 200 μm in diameter) were deposited through shadow mask e-beam evaporation. The final Pt/LBFO/NSTO FTJ devices of 10 μm in diameter were patterned by two-step photolithography with silicon dioxide (~100 nm SiO₂ on 300 μm thick silicon wafer) as the insulation layer. Microfabrication photoresist residuals on the surface of LBFO were cleaned by ozone plasma and inspected by AFM. The atomic layer structures were imaged using a transmission electron microscope (TEM, FEI Tecnai G2 F20). The surface phases (of different polarizations) imaging was obtained through piezoelectric force microscopy (PFM) with a Park NX-10 atomic force microscope (AFM). The conductive probes used in the PFM were Cr/Pt coated tips (Budget Sensors, Model: ContE-G). The measurements of current–voltage (I – V) and capacitance–voltage (C – V) were performed using Keysight B1500A Semiconductor Device Analyzer through a probe station. The pulse resistance measurements were conducted through a computer-controlled Keithley 2612 source meter and Rigol DG4062 waveform generator. The positive (negative) voltage is defined as the positive (negative) bias applied to the top Pt electrodes. A Lakeshore TTPX probe station and a JANIS VPF-100 cryostat were employed for low-temperature electrical measurements.

3. Results and discussion

The morphology and ferroelectricity of the LBFO ultra-thin films were characterized by AFM. In order to ensure its layered growth, a relatively slow growth rate of 1 nm/min was adopted. Fig. 1(a) shows the surface of 3 nm thick epitaxial LBFO film on the (001) facet of single-crystalline NSTO substrate with roughness R_a less than 0.4 nm (Fig. S1). Compared to island growth, layered growth tends to uniformly cover the substrate which can effectively reduce the probability of pinhole formation. The large square region in Fig. 1(b) was formed by

writing with a -5 V tip bias first, then flipping the voltage to $+5$ V to write and form the inner square region, which is imaged by PFM phase mapping. This result demonstrates the local ferroelectric polarization reversal of the LBFO layer. The measured PFM phase in the as-grown area is consistent with the region written by -5 V tip bias, which indicates the downward self-polarization. Since no morphological change has been found in the polarization reversed regions, local electrochemical reactions can be safely ruled out.

The epitaxial grown LBFO thin film has a well-aligned perovskite lattice structure implying a defect-free layer of LBFO/NSTO interface which is confirmed by TEM imaging. The Fast Fourier Transform (FFT) unveiled the in-plane compressive strain of LBFO layer, which is beneficial to maintain a high polarization [30,38]. All details of the above characterizations are included in the support information (Fig. S2). Since the LBFO layer in FTJ device is quite thin, it behaves as a zigzag type layered growth with unclear step boundary. We can see the neat lattice and sharp interface in the TEM measurements (Fig. S2), which demonstrates the layered growth from other perspectives.

To clarify the electric properties of the Pt/LBFO/NSTO devices, measurements of current and capacitance versus voltage (I – V and C – V) were performed using a semiconductor device analyzer together with a cryogenic probe station. A sketch of the device is shown in the inset of Fig. 2(b), where the diameter and thickness of the Pt top electrodes are 100 μm and 30 nm, respectively. The compliance current was set to 1 mA to avoid the possible thermal breakdown of the sample caused by Joule heating. The voltage sweeping during I – V measurement is from 0 to -8 V, then to 2 V, and back to 0 V, as shown in Fig. 2 (a). It is noticeable that the forward and backward I – V curves do not coincide at all measured temperatures, indicating the robustness of nonvolatile RS under the applied electric field. The sample can be set to a low resistance state (LRS) by applying a positive electric field or a high resistance state (HRS) through a negative electric field. A Schottky barrier forms at the interface even with a thin layer of LBFO due to the large work function difference between Pt and NSTO [43]. A clear diode-like current rectification is observed in the I – V curves, showing a much higher forward current than backward. Meanwhile, the absence of features of filament formation implies that this RS behavior is mainly due to the variation of the interface barrier rather than the generation and rupture of conductive filaments [12]. The linearity of the I – V curve of the Ag/NSTO/Ag junction indicates a good ohmic contact formation between NSTO and the probe station (shown in Fig. S3).

The Schottky barrier is identified by C – V measurements [28]. Fig. 2 (b) shows the capacitance versus voltage measurement at 1 kHz. Asymmetry of the measured C – V curves is induced by the Schottky barrier, and the butterfly shape is the typical feature of a ferroelectric capacitor. On the positive side, the capacitance decreases with

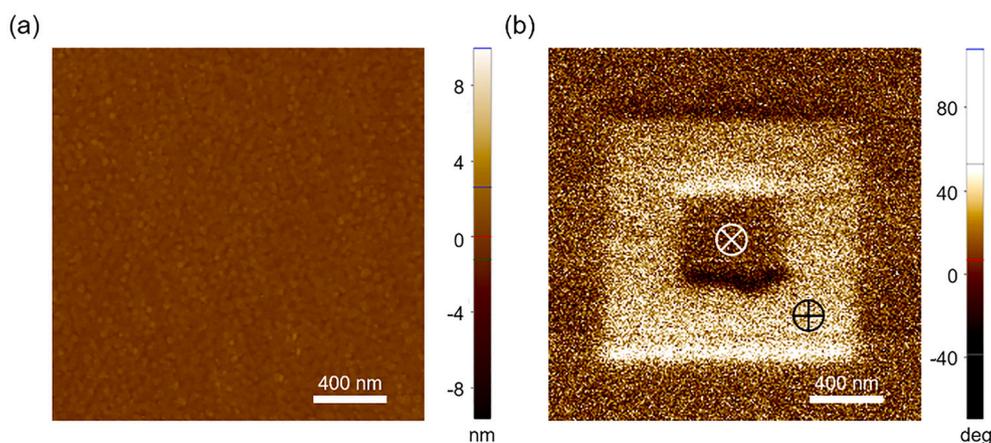


Fig. 1. (a) Morphology of the 3 nm thick epitaxial LBFO film on (001) NSTO substrate. (b) Corresponding out-of-plane PFM phase image after domain writing with -5 V tip bias in a $1.5 \times 1.5 \mu\text{m}^2$ area and then $+5$ V in the central $0.5 \times 0.5 \mu\text{m}^2$ square, represented by \oplus and \otimes .

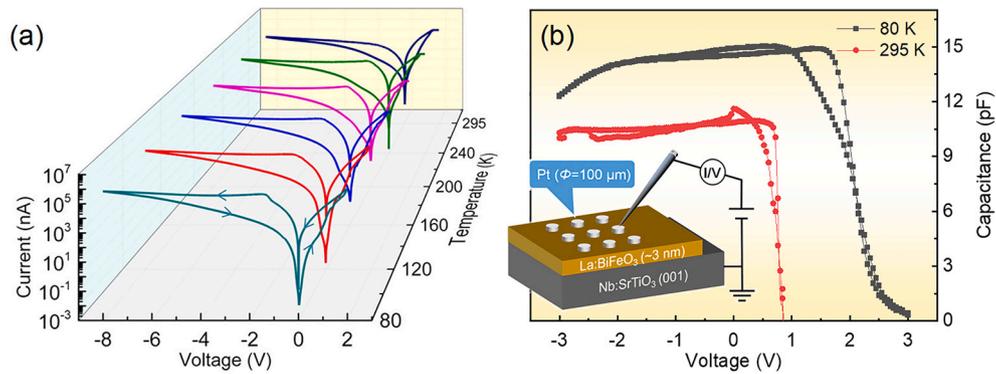


Fig. 2. (a) Semilogarithmic I – V curves of the Pt/LBFO/NSTO FTJs measured at different temperatures. (b) Capacitance versus voltage measurements at 80 and 295 K. Inset sketch the Pt/LBFO/NSTO FTJ devices.

increasing bias voltage, indicating that the Schottky barrier is gradually annihilated by electron accumulation. While on the negative side, the capacitance first increases up to a certain value then decreases rapidly, corresponding to the reverse-biased diode-like behavior observed in the I – V curves [23,44].

To gain more insight into the interfacial barrier dominated transport, a numerical fitting has been carried out on the measured curve of $G(V)/G(0)$ vs voltage. The excellent fitting of the normalized curves near 0 V (Fig. S5(a)) by parabolas indicates the applicability of the Brinkman–Dynes–Rowell (BDR) tunneling model [45]. Additionally, the symmetrical I – V curves and the weak temperature dependence of LRS (Fig. S5(b)) are also in accord with current tunneling. In the high bias regime, the linearity of $\ln(J/T^2)$ – V of HRS and LRS (Fig. S5(c) and (d)) implies that the transport current is mainly due to thermionic emission electrons. According to the linear relation of C^{-2} vs bias and larger slope of HRS than LRS, as shown in Fig. S6, we conclude that the observed RS behavior is mainly caused by the electrical tuning of the Schottky barrier. The transport of LRS is dominated by direct tunneling (DT) with a suppressed Schottky barrier. In contrast, the transport current of HRS results from thermionic emission (TE) through an enhanced Schottky barrier. These are consistent with the previous results of NSTO based FTJ devices [22,25,28,46].

The pulsed-read R – V measurement is a reliable way to characterize the nonvolatile RS properties in FTJs [20]. Fig. 3(a) shows the R – V loops measured with different voltages at room temperature, indicating typical multilevel RS behavior. As pointed by the arrows, a negative voltage applied to the Pt electrode will result in HRS and LRS when a positive voltage is applied. Pt/LBFO/NSTO FTJs show multilevel resistance transitions at different voltages. The switching ratio at ± 6 V can be more than 2×10^4 . For eliminating the interference of displacement current and capacitance, the time interval of each writing pulse was set to be 3 s. The remarkable similarity between the R – V curves and ferroelectric hysteresis indicates a strong correlation between them. To clarify the influence of pulse amplitude and width on the tunneling electro-resistance (TER), nonvolatile RS was measured with fixed opposite voltage pulses repeatedly. Stable and reversible resistance-switching with distinct multilevel resistance states are observed as shown in Fig. 3(b) and (c).

The LRS, as shown in Fig. 3(b), does not decrease monotonically with the increase of voltage, which can be detrimental to its accessibility. In principle, the switching time of ferroelectric induced RS could be as short as ~ 10 ns, but resistance switching charge trapping/de-trapping time is longer than 1 ms. [44] According to the results shown in Fig. 3(c), the onset time of RS is ~ 10 μ s, which indicates the contribution from

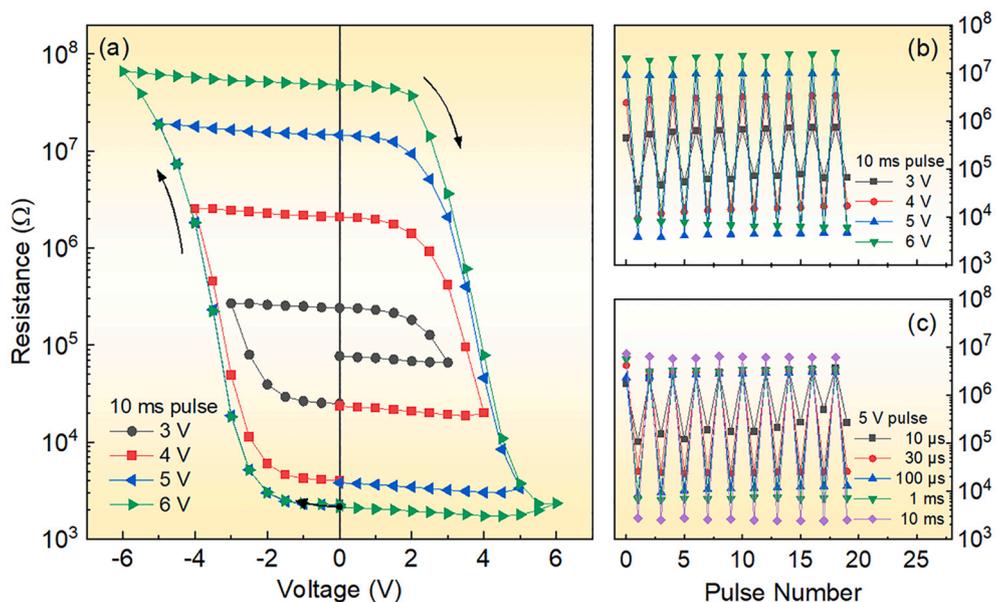


Fig. 3. Pulsed-read resistances measured at room temperature (a) continuous R – V loops measured with decreasing writing voltage amplitude. The black dot and arrows mark the starting point and writing sequence. (b) and (c) are amplitude and width dependent nonvolatile RS measurements.

those two mechanisms. A tentative interpretation is that the ferroelectric polarization reversal is usually accompanied by the displacement and formation of domain walls, which will speed up the release of trapped charges at the interface. Therefore, the RS switching in Pt/LBFO/NSTO FTJs could be explained by further accelerated trapping and de-trapping of charge via polarization reversal [32,47].

To examine the random accessibility of multilevel resistive states in Pt/LBFO/NSTO FTJs, random and opposite writing voltages were applied to set the multilevel resistance states (Fig. S7). In contrast to the modulation using fixed width and timing pulses, the resistances set by random pulses are significantly different. On one hand, in the random amplitude pulse modulation, the resistance states generated by the intermediate amplitude voltage have a large overlap, as shown in Fig. S7 (b). On the other hand, only HRSs overlap, while LRSs present clear and orderly stratification with random pulse width modulation (Fig. S7(d)). Note that the random pulse width-dependent measurements preliminarily demonstrate the feasibility of RAMNM in Pt/LBFO/NSTO FTJs.

Different from conductive filament type RS, the performance of interface type RS devices is closely related to their size. In these devices, energy consumption can be reduced and the switching speed can be increased by reducing lateral size, which is also beneficial for avoiding current leakage caused by pinholes and further increasing the switching ratio. Hence, we prepared a device with the Pt/LBFO/NSTO FTJ as shown in the inset of Fig. 4(a), where the top Pt electrodes with a diameter of 10 μm . Fig. 4(a) reflects the extremely high repeatability of the I – V property at room temperature, evidenced by the almost complete overlapped curves of cycled measurements from the device. As shown by the arrows, the direction and shape of I – V curves are consistent with the result in Fig. 2(a), but with more prominent RS features. The measured pulse width dependent R – V loops exhibit RS ratio up to 4×10^5 at room temperature, as shown in Fig. S8(a). Fig. S8 (b) shows the results of multilevel RS measurements with different pulse widths. The RS ratio decreases with pulse shortening. However, the

reversibility still holds even with pulses as narrow as 100 μs , failing at 10 μs . Multilevel resistive switching measurements were performed with randomly applied pulses of 3, 10, and 50 μs width, as shown in Fig. 4(b). Not only the distinct distribution of altered resistance states but also fast modulation speed has been reflected in Pt/LBFO/NSTO FTJ devices. To better understand the performance of Pt/LBFO/NSTO FTJ, the retention property and the temperature dependence of HRS/LRS have been measured. In the retention tests, the HRS remains nearly unchanged for the whole measured period of more than an hour, as shown in Fig. 4(c). While relaxation is observed in LRS and it slowly increases with time. After more than 1 h, the RS ratio of Pt/LBFO/NSTO FTJs is still above 3×10^3 , revealing its robust retentivity at room temperature. In the R – T curves (Fig. S9(c)), LRS increases rapidly with the increase of temperature, showing a tendency toward metal-like behavior. With the temperature increase, HRS first stays constant and then decreases rapidly. The metallicity of LRS can be understood as the diffusion of interfacial charged defects caused by thermal fluctuations and the decrease of the potential barrier. Ferroelectric bound charges can remain stable below the Curie temperature, while interfacial trapped charges are more sensitive to thermal perturbations. These results show the significant contribution of trapped charges to the variation of the interfacial barrier. Cycling measurements were performed at 80 K and room temperature. As shown in Fig. 4(d), almost no observable degradation is observed after cycling more than 2000 times with a switching ratio above 2×10^5 at 80 K. The HRS remains constant, and the LRS shows a slight fluctuation over time at room temperature, as can be seen in Fig. S9(d). These results indicate the feasibility of realizing a four-state-memory through tuning the pulse width of ± 5 V.

The pulse width-dependent measurements evidenced the random accessibility of the multilevel LRS and overlapped HRS. These results beg the question: Why is there a significant difference in the random modulation of amplitude and pulse width-dependent resistance? To elucidate the physical mechanism, schematic band diagrams of HRS and

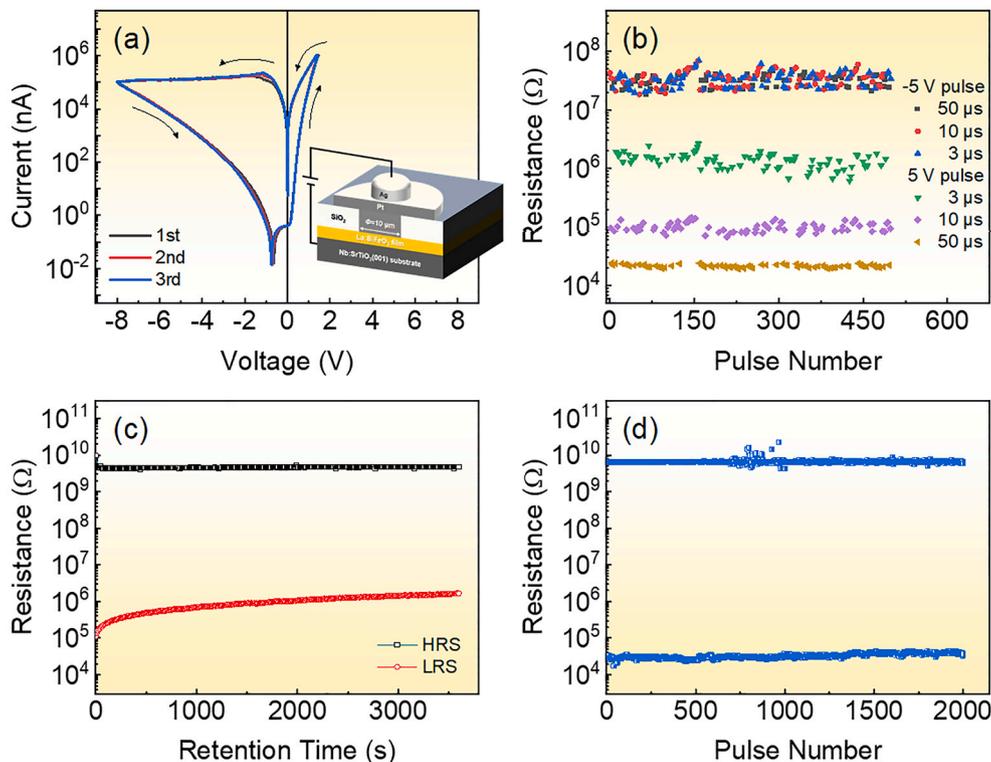


Fig. 4. Electrical measurements of the Pt/LBFO/NSTO FTJ devices at room temperature (a) Semi-log I – V curves in continuous measurement. (b) Resistance distribution after a pulse sequence with random pulse widths. The reading voltage is -0.2 V. (c) Resistance retention tests at 295 K. (d) Repeatability measurements by ± 8 V, 100 ms pulses and -0.5 V read voltage at 80 K.

LRS are sketched in Fig. 5. Due to the electrostatic interaction, the charge accumulation and depletion near the interface will be affected by bond charges such as polarization charges or charge defects, namely interface charge coupling. Oxygen vacancies (V_O) usually gather at the surface of oxide films because of the reduction of formation energy. These V_O act as deep traps for electrons, when lower the Fermi level, they can release electrons to the conduction band, and become positively charged V_O^+ and V_O^{2+} . Under a weak electrical field, the polarization and charged defects are both localized charges, which affect the distribution of free carriers and the band diagram. While a high electrical field will redistribute the bond charges, thus changing the interfacial barrier. So, the bias could modulate trapped charges and polarization, which changes the interfacial barrier and the forms HRS and LRS. The difference between the polarization charge and charged defects are the ferroelectric coercive field (E_c) and remanent polarization (P_r), which will strengthen the device's nonvolatility.

The work function of Pt is 5.65 eV, the bandgap and electron affinity of NSTO are 3.2 eV and 4.0 eV, respectively [34,48]. Like many other NSTO based devices, Pt/LBFO/NSTO FTJ shows typical memristive features. However, due to complex interfacial charge coupling in random modulation, the activation energy of trapped charges varies. It constrains the effect of amplitude-dependent modulation, which is not the case for the width-dependent modulation, where the limitation is the number of flowing charges. The transport in HRS is based on hot electron emission, which is less sensitive to the shape of the Schottky barrier. In contrast, the direct tunneling in LRS can be significantly affected by the height of the Schottky barrier, which is closely related to the interfacial bound charges. Therefore, pulse width modulation can ensure the stability of different LRS in the random process by accurately controlling the quantity of released interfacial charges.

4. Conclusions

In summary, high-performance memristive Pt/LBFO/NSTO FTJs have been fabricated using magnetron sputtering deposition and microfabrication techniques. More importantly, the feasibility of RAMNM has been demonstrated in such devices with random pulse width modulation. The obtained RS ratio can be as high as 10^5 , which provides an adequate continuous window for multilevel memory. A tentative mechanism of the RAMNM in Pt/LBFO/NSTO FTJs is proposed by comparing results between different random pulse modulations. The combination of this device structure design and operation mode provides a promising route to develop high-density memristive devices. This result demonstrates the feasibility of random modulation and accessibility of multilevel nonvolatile memory, which is crucial for the practical application of RAMNM.

CRedit authorship contribution statement

Dong Li: Methodology, Investigation, Data curation, Writing – original draft. **Xiaodong Zhu:** Data curation, Writing – review & editing. **Yanan Wu:** Investigation, Writing – review & editing. **Jian Zhao:** Methodology, Data curation. **Kaimin Zhang:** Methodology, Data curation. **Rui Li:** Methodology. **Danni Hao:** Methodology. **Yanqing Ma:** Validation, Writing – review & editing. **Ramiro Moro:** Writing – review & editing. **Lei Ma:** Conceptualization, Supervision, Methodology, Validation, Writing – review & editing, Funding acquisition, Project administration.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

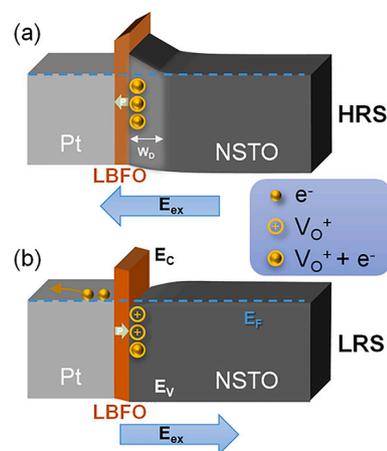


Fig. 5. Schematic band diagrams for (a) HRS and (b) LRS of Pt/LBFO/NSTO FTJs. E_{ex} is the external electrical field; W_D is the width of the depletion layer; E_V , E_F , and E_C represent the position of the valence band, Fermi level, and conduction band, respectively.

Data availability

Data will be made available on request.

Acknowledgments

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Appendix A. Supplementary data

See the supplementary material for the morphology of the 3 nm thick epitaxial LBFO film; TEM image and FFT results of La:BiFeO₃ (LBFO) on top of single-crystalline Nb:SrTiO₃ (NSTO); $I-V$ curve of the Ag/NSTO/Ag structure; fitted $I-V$, $C-V$ curves, pulsed read $R-V$ and repeatability measurements in Pt/LBFO/NSTO FTJ devices. Supplementary data to this article can be found online at [<https://doi.org/10.1016/j.mee.2022.111908>].

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