A simple yet high-performance position-sensitive detector with readout electronics

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ABSTRACT

Lowering the manufacturing complexity of position-sensitive detectors (PSDs) while retaining their performance has always been challenging. Here we introduce a delay-line PSD for direct usage in charged ion beam detection. The system fully constructed using Printed Circuit Board Assembly (PCBA) greatly reduces manufacturing complexity while maintaining excellent detection performance. A structurally simple and stable serpentine delay-line anode was fabricated using commercially available Printed Circuit Board (PCB). Combined with Constant Fraction Discriminators (CFDs) based high-precision readout electronics and a Field Programmable Gate Array (FPGA) chip, the system achieves Full Width at Half Maximum (FWHM) resolutions of 210 μm and 350 μm along the X and Y axes, respectively.

I. INTRODUCTION

The detection of positional information is crucial for analyzing the spatial distribution of particles such as photons, neutrons, and electrons, as well as for determining the position of particle beams. Therefore, Position-sensitive detectors (PSDs) serve as a core device in all these studies.[1-8] The mainstream type of PSDs include: phosphor screen imaging detectors,[9, 10] which are highly dependent on the performance of Charge Coupled Device (CCD) cameras; semiconductor detectors like Timepix,[11, 12] offering high resolution but having a complex structure; and electronics-based delay-line PSDs which has the best balance between structural complexity and performance.[13-15]

The delay-line PSD consists of two components: delay-line anode and readout electronics. The delay-line anode originates from the planar zigzag delay-line anode designed by Lampton *et al.*,[16] which is able to acquire positional information in one dimension through time delay. Later, Sobottka *et al.* proposed the crossed delay-line

anode design[17] which was fabricated by wire-winding. This anode obtains the positional information of incident particles by measuring the time delay along the mutually perpendicular coordinate axes. In 1995, the first serpentine delay-line anode was fabricated by Friedman *et al.* by laser cutting circuit boards.[18] About five years later, Lampton *et al.* improved the serpentine delay-line anode by holes drilling instead which makes, the two crossed lines receiving charged particles on the same plane become possible.[19]

Both conventional Wire-winding and laser cutting PCB not only require rather expensive equipment but also are time consuming. Furthermore, the circuit board substrate may undergo carbonization during the laser ablation process, which places stringent requirements on the substrate material. Moreover, copper particles generated during the ablation process may also shorten the insulation channels.

A perfect impedance matching between data extraction circuit and the delay-line PSD is essential.[20, 21]. For instance, a recently reported Microchannel Plate (MCP) delay-line detector combo from RoentDek GmbH[22] has a Full Width at Half Maximum (FWHM) resolutions of only 460 μm and 579 μm along the X and Y axes, respectively, which manifests an incomplete exploitation of the detector's capabilities due to the imperfect impedance matching.[23] If the devices other than the MCP are manufactured using the same method, and the removal of redundant connectors between the readout electronics and the receiving anode is achieved, this will greatly simplify the manufacturing complexity of the PSDs and avoid the noise introduced by the connectors.

Here, we constructed a chemically etched Printed Circuit Board (PCB) as serpentine delay-line anode for a PSD. It ensures structural stability and enables the batch fabrication of multiple anodes, thereby improving production efficiency. Furthermore, a Constant Fraction Discriminators (CFDs) and Field Programmable Gate Array (FPGA) chip based readout electronics board was developed. Both of them are fully fabricated using printed circuit board assembly (PCBA), giving them the potential to be manufactured on one PCB in the future. Experiments indicate that although they have a simple manufacturing structure, they maintain excellent resolution and can be directly applied to the detection of charged ion beams.

II. DESIGN

The block diagram of the designed PSD and readout electronics is shown in Fig.1. The serpentine delay-line anode is implemented on a chemically etched PCB, the readout electronics includes sampling amplifier circuits, CFDs, and an FPGA chip. When charged particles strike on the anode, two pairs of electrical pulses are created with the position information of X1/X2 and Y1/Y2. Then, these signals are processed

by the readout electronics to rebuild the particle strike positions.

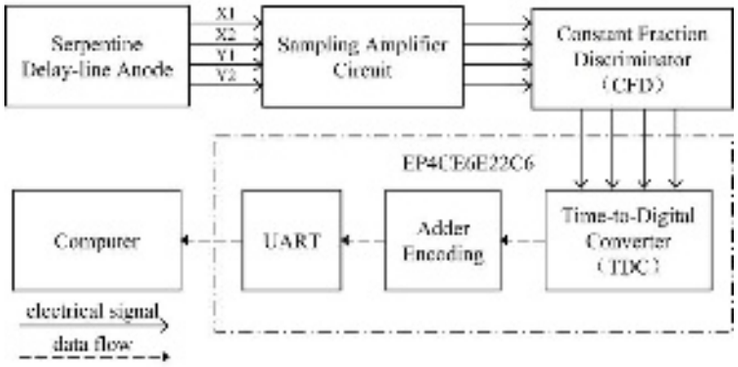

Fig.1. Diagram of the system architecture. The solid line represents the electrical signal path, and the dotted line represents the data flow path. Function blocks inside the dotted-dashed line are the parts of FPGA chip.

As shown in Fig. 2(a), the serpentine delay-line anode features a gold-plated copper conductor in its central region to receive charged particles. The exposed area of this conductor is 74.4 mm * 74.4 mm and can be adjusted as required. This region incorporates the top-layer delay-line, and collector-plates connected to the buried-layer delay-line through vias. As shown in Fig. 2(c), a single serpentine delay-line anode comprises four conductive layers, arranged sequentially as follows: top-layer delay-line with a shielding ground layer under it, followed by a buried-layer delay-line and another shielding ground layer under it. These layers, after fabrication, are laminated and assembled using photo-curing technique and are isolated from each other with insulators. The fabricated serpentine delay-line anode employs FR-4, one of the most commonly used insulating material. The operating principle of the serpentine delay-line anode is described in detail in Section II A.

Fig. 2(b) shows the readout electronics board. Here, OPA694 based sampling amplifier circuits and OPA2652 and MAX9601 based CFDs are sequentially arranged from the top and bottom layers of the circuit board; while an FPGA chip (EP4CE6E22C6, Altera) based dual function circuit for both time digitizing and readout is located along the central axis of the circuit board. Signals output from the serpentine delay-line anode are input via the SMA connector on the left side, and processed sequentially by the sampling amplifier circuits, CFDs, and the FPGA chip. The processed results are output via the USB-B connector to the computer. Additionally, a BNC connector on the right side is used to receive an additional external trigger signal. The Time-to-Digital Converter (TDC) algorithm is described in Section II B. It is implemented within the FPGA chip, rather than being realized with discrete analog circuitry.

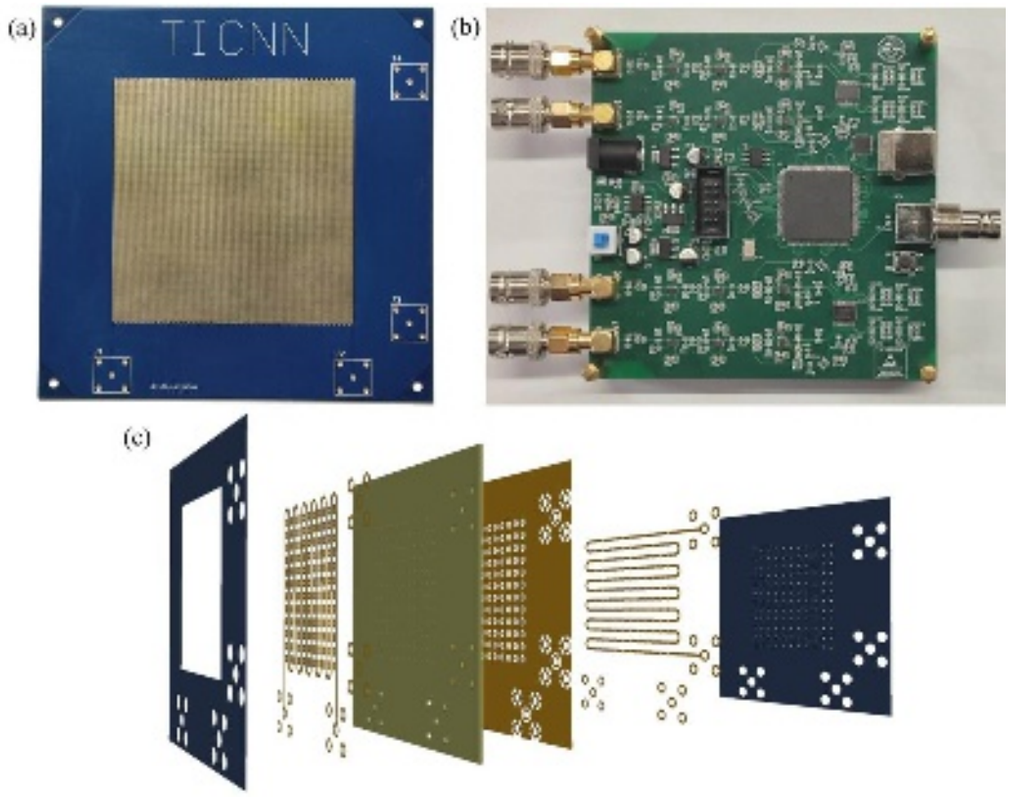

Fig. 2. Photos of a delay-line anode, readout PCB board and 3D model of the delay-line anode. (a) Photo of the serpentine delay-line anode. (b) The readout electronics board. (c) Exploded-view of the serpentine delay-line anode, simplified to show only the distinct layers, they are, from the left to the right, solder mask, top delay-line, dielectric layer, shield ground plane, buried delay-line, and the solder mask.

A. Details of Serpentine Delay-line Anode

Charged particles striking on the serpentine delay-line anode generate current pulses. These pulses propagate along the lines in both directions, originating from the impacting point. Fig. 3 shows a schematic diagram of the top-layer delay-line that is responsible for position sensing along the X-axis, and the buried-layer delay-line that is responsible for position sensing along the Y-axis and perpendicular to the X-axis. In the diagram, the shielding ground layers are hidden. Among the four output signals, the first to arrive is designated as the timing reference. Concurrently, timing measurements are performed within the time window defined by the signal's propagation delay along the buried serpentine delay-line.

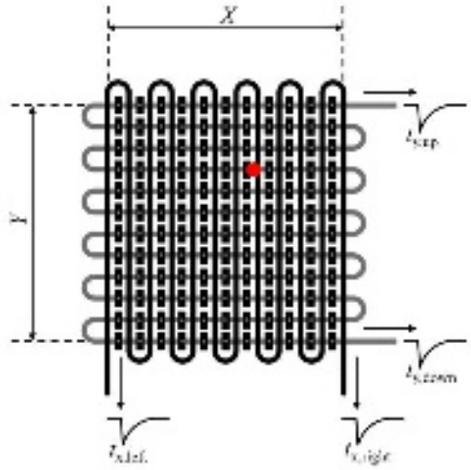

Fig. 3. Schematic diagram of a serpentine delay-line anode. Black regions: Top-layer delay-line and collector-plates. Gray regions: Buried-layer delay-line and vias. Red dots: Charged particle beam strike location.

For example, in position sensing along the X-axis:

(i) Determine whether the output signals of the top-layer delay-line originate from the same incident charged particle event:[24]

$$T = \frac{L_x\sqrt{\varepsilon_r}}{c} = t_{x,left} + t_{x,right} \tag{1}$$

Where T is the measured total time delay from the top-layer delay-line, L_x is the total path length of the top-layer delay-line, ε_r is the dielectric constant of the insulating substrate in the circuit board, c is the speed of light, $t_{x,left}$ and $t_{x,right}$ are the measured arriving time of signals from left and right end of the top-layer delay-line respectively.

(ii) Calculate the arrival time difference (Δt) between the two output signals at left and right end of the top-layer delay-line.

$$\Delta t = t_{x,left} - t_{x,right} \tag{2}$$

(iii) Convert Δt to the distance between the charged particle incident point and the central point of the serpentine delay-line anode, so the position x of the incident point along the X-axis can be described as following equation (3):

$$x = X_m + 2f\Delta t\frac{cX}{L_x\sqrt{\varepsilon_r}} \tag{3}$$

where X_m is the coordinate of the central point of the serpentine delay-line anode along the X-axis, X is the width as defined in Fig. 3, and the correction coefficient f, used for calibrating reconstructed positions, is back-calculated from pulse signals injected at the four vertices of a rectangular area defined within the X and Y ranges in

Fig. 3, using a needle tip.

In electronic design, 50 Ω is one of the commonly used characteristic impedances. As such, both the anode and the readout electronics in this work feature 50 Ω terminations. However, the serpentine delay-line anode has different impedance across different layers: the top-layer delay-line follows the microstrip model, whereas the buried-layer delay-line follows the stripline model. To achieve approximate 50 Ω impedance matching requirements for both, the top-layer delay-line was set to linewidth of 0.25 mm and line space of 0.55 mm, while the buried-layer delay-line adopted a width of 0.15 mm and line space of 0.65 mm to balances the cost and yield under conventional manufacturing processes. The impedance can be calculated as following equations (4) and (5).[25]

$$Z_m = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \tag{4}$$

$$Z_s = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{5.98(D + T)}{\pi(0.8W + T)}\right] \tag{5}$$

Where Z_m is the microstrip impedance, Z_s is the stripline impedance, H is the distance between the top-layer delay-line and the shielding ground layer, T is the copper thickness of the lines, W is the line width, and D is the distance between the two shielding ground layers.

B. Details of TDC

The TDC implements time measurement by combining coarse timing from a counter with fine timing from a carry chain. As shown in Fig. 4(a), the coarse timing clock for the counter is derived from the reference clock. When signals arrive at both ends of a line, the carry chain subdivides the coarse timing period, thereby achieving high-resolution time measurement. The time interval between the signals can be calculated using the following equation (6), where n is a positive integer and $t_{interval} \le T_{ref}$.

$$t_{interval} = (2 + n)T_{coarse} + t_{fine1} - t_{fine2} \tag{6}$$

The fine time measurement is obtained by combining the position of completed adder logic elements (LEs) within the chain with the time span per LE. As shown in Fig. 4(b), when a signal arrives, a carry signal propagates sequentially through the chain of LEs. Upon the rising edge of the next coarse timing cycle (CLK_240MHz), the operational results of all adders are latched for outputting. The carry chain is constructed with 128 LEs and fully covers a single coarse timing period, exhibiting an output pattern characterized by "1...111100...0". The position of the 0-to-1 transition indicates the location of the transmitted signal.

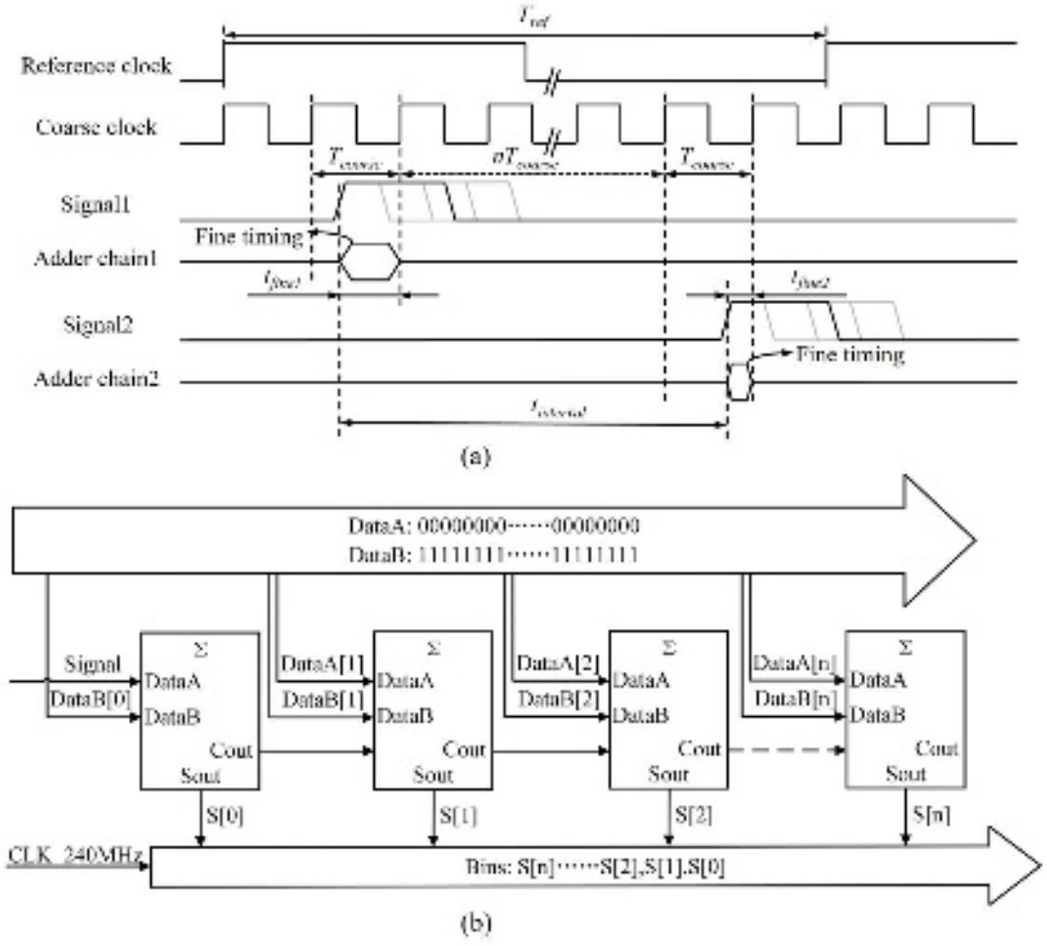

Fig. 4. Diagram of the interval measurement method. (a) Timing sequence diagram of the input signals and measured time. (b) Diagram of the fine time measurement circuit.

III. EXPERIMENTAL TEST

The test includes three parts: serpentine delay-line anode test, readout electronics test, and delay-line detector test. Electron beams are generated by an oscilloscope electron gun, which was installed horizontally in a homemade vacuum chamber, with its original beam shaping and manipulating electrodes and power supplies. A small aperture made of thick aluminum foil was positioned opposite the electron gun to serve as a beam collimate, when the beam running at scanning mode the continuous beam will be converted into a sequence of discrete beam bunches since the existence of this aperture.

A. Serpentine Delay-line Anode Test

In our experiments, short circuits were observed in serpentine delay-line anodes made by laser ablation, which might be caused by substrate carbonization or copper powder deposition. The chemical etching method avoided this issue. Fig. 5 shows the signals from an anode made by chemical etching, the buried-layer delay-line shows

approximately 65% strength of the top-layer delay-line.

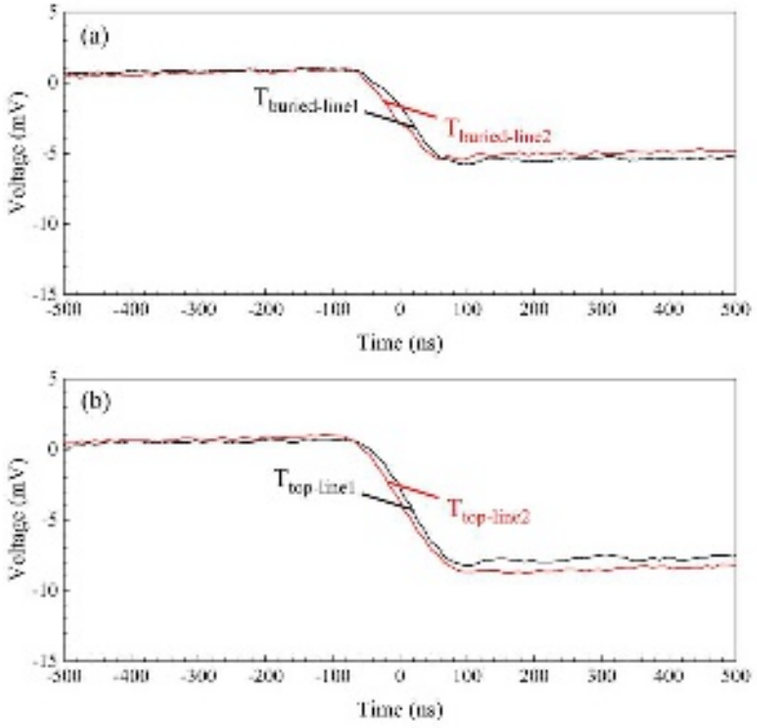

Fig. 5. Response of the serpentine delay-line anode to the electron beam, measured on the oscilloscope. (a) Outputs from both ends of the buried-layer delay-line. (b) Outputs from both ends of the top-layer delay-line.

B. Readout Electronics Test

Xilinx's FPGA chips incorporate CARRY4 logics, which feature short-chain function and are predominantly utilized in existing FPGA-based TDC implementations. However, the number of available CARRY4 logics is limited. The Altera EP4CE6E22C6 is employed in our design, comparing with equivalent-grade chips from Xilinx it has much lower cost. Although the delay per LE of this Altera chip longer than that of a CARRY4 logic in Xilinx FPGAs, carry chains constructed from these LEs can nevertheless be extended while maintaining delay uniformity. The carry chains within the readout electronics were tested using numerous signals from a pulse generator (Stanford, DG645). Fig. 6 shows the cumulative results and the statistical analysis of the time distribution. The slope of the fitting curve demonstrates that the average propagation delay per LE in the carry chain is less than 47 ps.

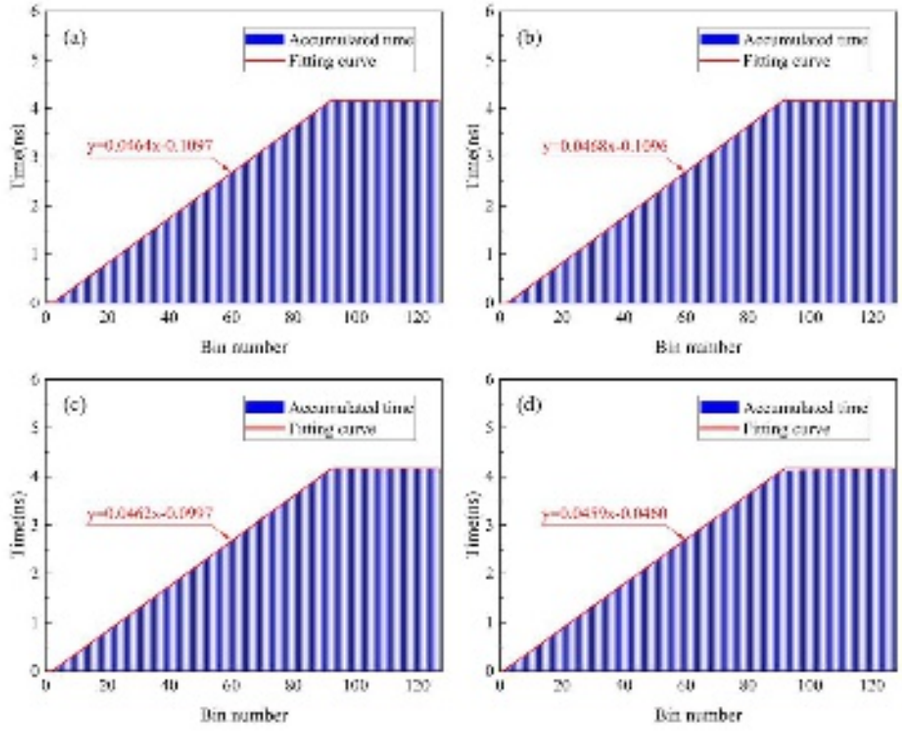

Fig. 6. Accumulated fine timing results allocated by code density. (a) Channel #1: Adders 4 to 94 are used. (b) Channel #2: Adders 4 to 93 are used. (c) Channel #3: Adders 4 to 94 are used. (d) Channel #4: Adders 3 to 93 are used.

C. Delay-line Detector Test

To evaluate the performance of the serpentine delay-line anode coupled with the readout electronics, tests were conducted using an aluminum foil mask with apertures approximately 0.7 mm in diameter as a collimator. The apertures on the mask are positioned at points defined by the detector's central axis and at a displacement of ± 20 mm from it. As shown in Fig. 7, the PSD achieved FWHM resolutions of beam spot of 210 μm and 350 μm along the X and Y axes, respectively. These resolutions are primarily limited by the intensity and divergence of the test electron beam. The timing accuracy of the CFD is closely related to the rise time of the signal edge, a steeper signal edge results in higher timing precision.[26, 27] However, to avoid burning the fluorescent screen, the electron beam current in the oscilloscope electron gun is kept low. Therefore, in the practical test setup, the best achievable signal rise time that satisfies the test requirements for signal amplitude is approximately 120 ns, as shown in Fig. 5. Although the obtained values still demonstrate the excellent performance of the system, it should be noted that the measurement could achieve better resolution if the experimental platform were equipped with a higher-quality charged particle beam source.

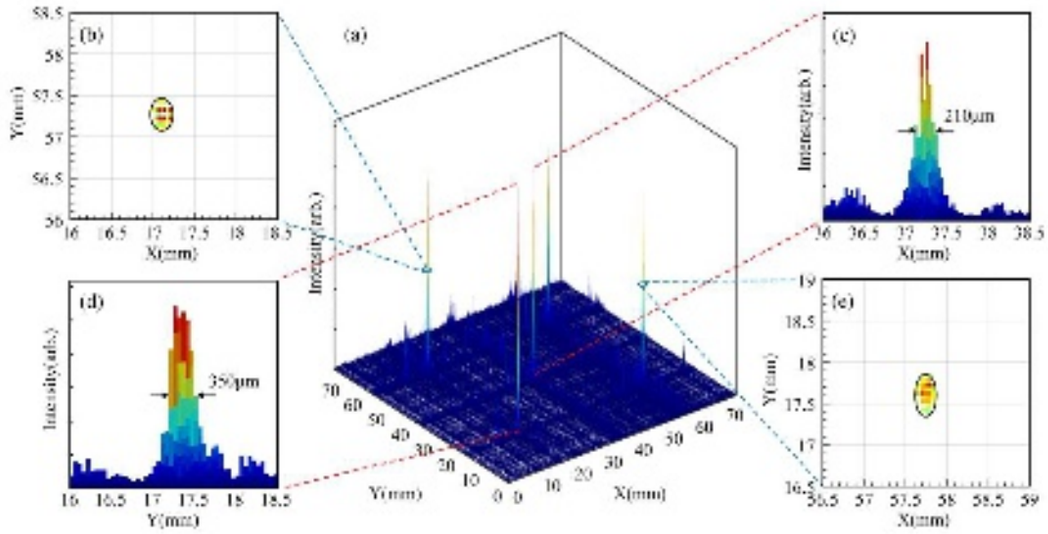

Fig. 7. Reconstructed electron-beam impact locations. (a) 3D spatial distribution of detected electron-beam impact positions. (b, e) X-Y projection of reconstructed image FWHM contours. (c) X-axis projection. (d) Y-axis projection.

IV. CONCLUSION

This paper presents a PSD with readout electronics. Its serpentine delay-line anode was fabricated using commercially available chemically etched PCB. The coupled readout electronics, implemented with CFDs and an FPGA chip, accomplishes high-precision signal readout and digitization of anode outputs. The direct tests with an oscilloscope electron gun, the readout electronics achieved an average time resolution of less than 47 ps, and the detector achieved FWHM spatial resolutions of 210 μm and 350 μm along the X and Y axes, respectively. Compared with the conventional delay-line detector design, this approach largely reduces both fabrication challenge as well as reaching high spatial resolution.

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Author Contributions:

Tianjin Ma: Methodology, Investigation, Data curation, Carrying out experiments, Writing–original draft preparation.

Xiaohan Wang: Methodology, Investigation, Carrying out experiments.

Zhi Chen: Methodology, theoretical simulation.

Jinhong Huang: Investigation, Data curation.

Lei Ma: Conceptualization, Methodology, Funding acquisition, Supervision, Writing- review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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